TITAN MICRO® ELECTRONICS

1/2/4Gbit SPI NAND Product Specification

Contents

1. GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra-cost effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI-NOR and standard parallel NAND Flash, with advanced features:

- Total pin count is 8, including VCC and GND
- Density 1/2/4Gb
- Superior write performance and cost per bit over SPI-NOR
- Significant low cost than parallel NAND

This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pin out from one density to another. The command sets resemble common SPI-NOR command sets, modified to handle NAND specific functions and added new features. SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

- **User-selectable internal ECC**. ECC parity is generated internally during a page program operation. When a page is read to the cache register, the ECC parity is detected and corrects the errors when necessary. The device outputs corrected data and returns an ECC error status.

- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data. This command string can only be used on blocks with the same parity attribute.

- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correct by internal ECC when ECC enabled.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

2. FEATURE

◆ 1/2/4Gb SLC NAND Flash

◆Flash Size

Flash size: 1Gb/2Gb
Page size: (2048+128)byte
Block size: (128K+8K) byte

Flash size: 4Gb:
Page size: (4096+256) byte,
Block size: (256K+16K) byte

◆ Standard, Dual, Quad SPI

- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3
- 3.3V: 104MHz for fast read with 30pF load
- 3.3V: Dual I/O Data transfer up to 208Mbits/s
- 3.3V: Quad I/O Data transfer up to 416Mbits/s

◆ Software/Hardware Write Protection

- Write protect all/portion of memory via software Register protection with WP# Pin

◆ Single Power Supply Voltage

- Full voltage range for 3.3V: 2.7V ~ 3.6V

◆ Advanced security Features

- 10 page ,2K-Byte OTP Region

◆ Program/Erase/Read Speed

- Page Program time: 600us typical
- Cache Program time: 20us minimum
- Block Erase time: 3ms maximum
- Random page read time: 280us typical
- Sequence page read/Cache read time: 20us minimum

◆ Low Power Consumption

- 30mA typical erase/program current
- 10mA typical active current
- 65uA typical standby current
- 35uA typical deep power-down current

◆ Enhanced access performance

- 2Kbyte cache for fast random read
- Cache read and cache program

◆ Temperature

- Operation: -40℃ to 85℃
- Storage: -65℃ to 150℃

◆ Reliability

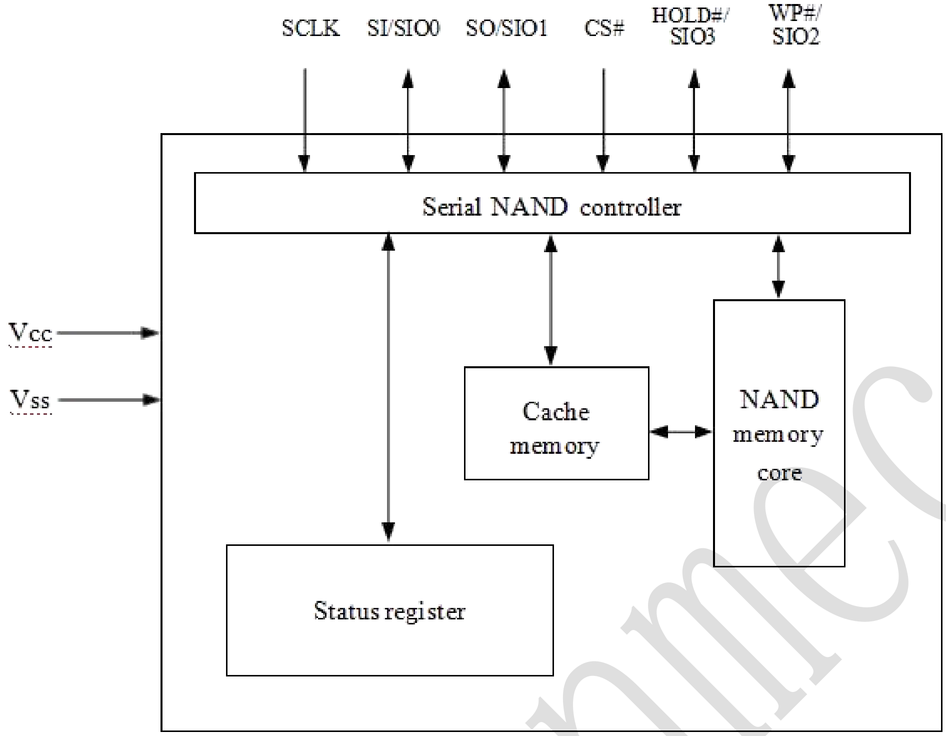
- P/E cycles with ECC: 100K
- Data retention: 10 Years

◆ Internal ECC[(1)]

- 8bits/528byte

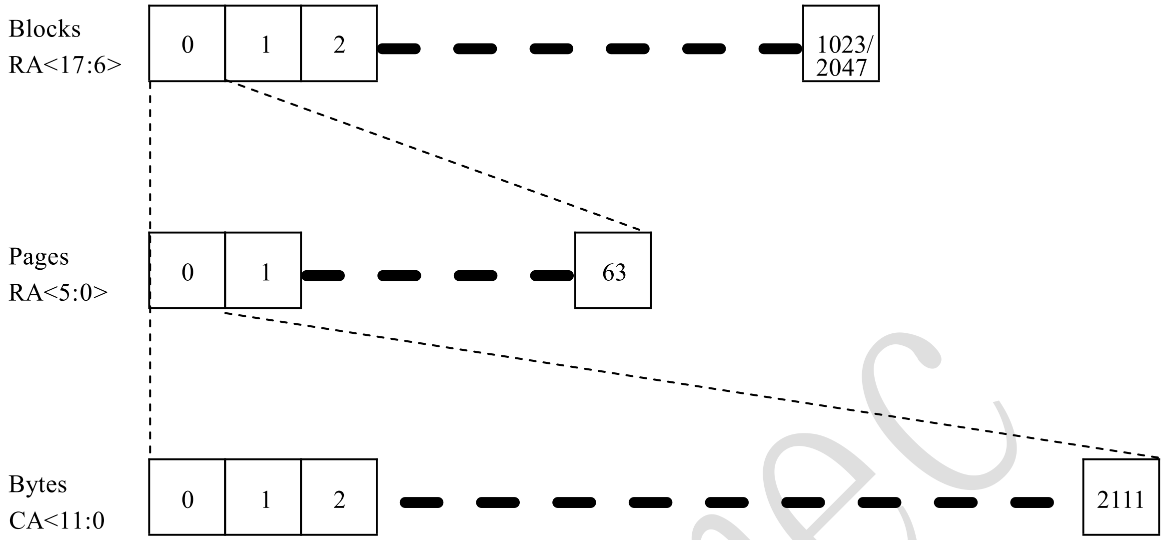
Note:
(1). ECC is on default, which can be disable by user.

3. BLOCK DIAGRAM



4. MEMORY MAPPING

For 1/2Gb

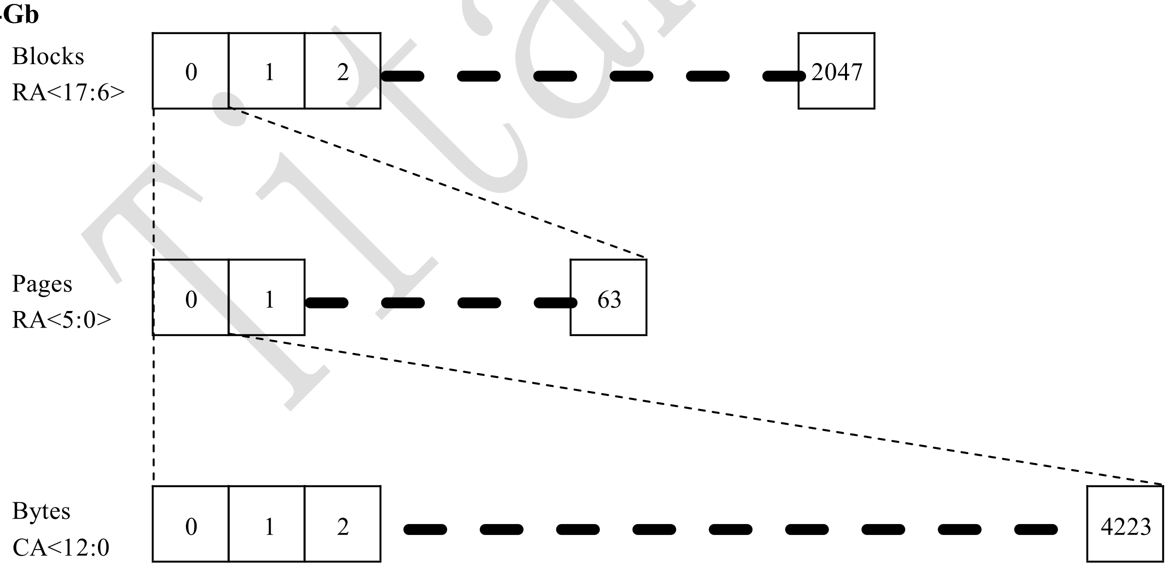


Note:

1.CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds,” do not exist in the device and cannot be addressed.

2. RA: Row Address. RA<5:0>selects a page inside a block, and RA<17:6>selects a block.

For 4Gb



Note:

1. CA: Column Address. The 13-bit address is capable of addressing from 0 to 8191 bytes; however, only bytes 0 through 4223 are valid. Bytes 4224 through 8191 of each page are “out of bounds,” do not exist in the device and cannot be addressed.

2. RA: Row Address. RA<5:0>selects a page inside a block, and RA<17:6>selects a block.

5. ARRAY ORGANIZATION

TM1F1GUAI			
Each device has **1Gb**	**Each block has**	**Each page has**	**Unit**
128M + 4M	128K+8K	2K+128	bytes
1024 x 64	64	-	pages
1024	-	-	blocks

TM1F2GUAI			
Each device has **2Gb**	**Each block has**	**Each page has**	**Unit**
256M+8M	128K+8K	2K+128	bytes
2048 x 64	64	-	pages
2048	-	-	blocks

TM1F4GUAI			
Each device has **4Gb**	**Each block has**	**Each page has**	**Unit**
512M+16M	256K+16K	4K+256	bytes
2048 x 64	64	-	pages
2048	-	-	blocks

6. FTL Engine(Optional)

TM1FxxxUXX have the FTL engine to provide more advance features.Hereunder is the additional highlight items for application.

1. TM1FxxxUXX provide several important features

• Randomizer: TM1FxxxUXX has the randomizer to convert the data into the average distribution of zero and one in advance to solve the chance of misjudgment of data.

• FTL : TM1FxxxUXX has FTL to do wear Leveling and can do bad block management.

2. Reserve 40 blocks for FTL engine.
3. Address Mapping

Bad blocks can be configured to be distributed at the end of the physical address space. This allows the host to obtain a contiguous logical address space, thereby eliminating the need for host-side bad block management procedures. Simultaneously, the system also supports random mapping of bad blocks across any physical location.

4. Supports NOR-like operations, including

• Compatibility with 03h and 0Bh commands (standard SPI NOR read commands)

• Configurable dummy clock cycles (up to 32 cycles, exceeding the typical 4-cycle limit of raw NAND)

• Byte-addressable programming: Writes can target any single byte (unlike native NAND's 512+16/32-byte page write requirement)

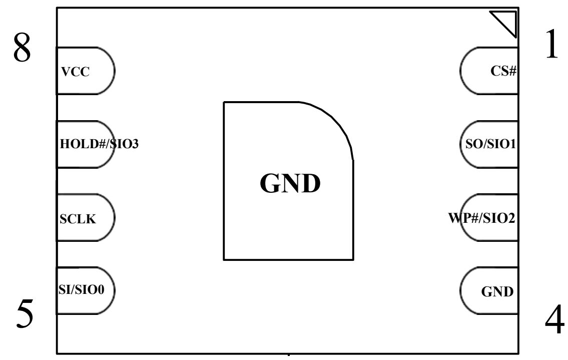
• In-place data modification: Allows direct overwriting of existing data (similar to NOR flash)

This design significantly reduces migration complexity when transitioning from SPI NOR to SPI NAND by emulating NOR flash behavior.

5. When using FTL, ECC functionality is mandatorily enabled. While meeting customer OOB (Out-of-Band) requirements, the ECC error correction capability is maximized to the greatest extent possible.

Note: FTL engine is only available in version B.

7. PIN DESCRIPTION



Bottom View

Pin Name	I/O	Description
CS#(1)	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
GND	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD# /SIO3	**I/O**	Hold Input, active low/Serial Data Input Output 3
VCC	**Supply**	Power Supply

Note:

(1) CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

8. DEVICE OPERATION

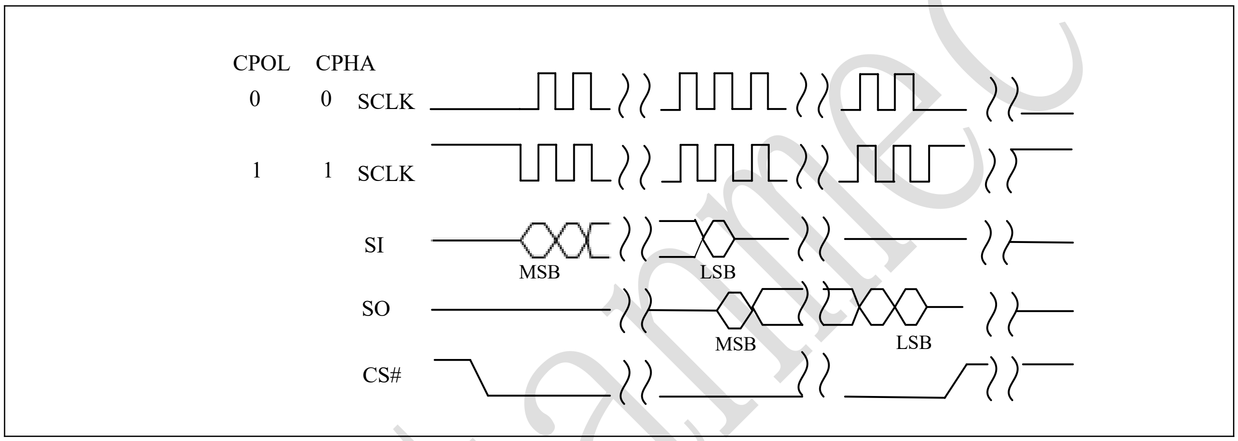
8.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes. All timing diagrams shown in this data sheet are mode 0. See **SPI Modes Timing Diagram** for more details.

SPI Modes Timing Diagram



Note:

- While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3). Do not toggle SCLK until CS# is driven LOW.
- We recommend that the user pull CS# to high when user don't use SPI flash, otherwise the flash is always in the read state, which is not good for flash.
- When CS# is high and SCLK at VCC or GND state, the device is in idle state.

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

8.2 HOLD Mode

The HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of reading, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

8.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being over written. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

To enable the Write Protection, the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

9. COMMANDS DESCRIPTION

9.1 Commands Set table

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Get Features	0FH	A7-0	D7-0	D7-0	D7-0	D7-0	D7-0	D7-0	D7-0
Set Feature	1FH	A7-0	D7-0						
Read ID	9FH	Dummy	MID	DID1	DID2				
Page Read (to cache)	13H	PA23-16	PA15-8	PA7-0					
Read	03H	CA15-8	CA7-0	Dummy	D7-0	D7-0	D7-0	D7-0	D7-0
Fast Read	0BH	CA15-8	CA7-0	Dummy	D7-0	D7-0	D7-0	D7-0	D7-0
Fast Read with 4-Byte Address	0CH	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-0	D7-0	D7-0
Fast Read x 2	3BH	CA15-8	CA7-0	Dummy	D7-0 / 2	D7-0 / 2	D7-0 / 2	D7-0 / 2	D7-0 / 2
Fast Read x 2 with 4-Byte Address	3CH	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-0 / 2	D7-0 / 2	D7-0 / 2
Fast Read x 4	6BH	CA15-8	CA7-0	Dummy	D7-0 / 4	D7-0 / 4	D7-0 / 4	D7-0 / 4	D7-0 / 4
Fast Read x 4 with 4-Byte Address	6CH	CA15-8	CA7-0	Dummy	Dummy	Dummy	D7-0 / 4	D7-0 / 4	D7-0 / 4
Fast Read Dual IO	BBH	CA15-8 / 2	CA7-0 / 2	Dummy /2	D7-0 / 2	D7-0 / 2	D7-0 / 2	D7-0 / 2	D7-0 / 2
Fast Read Dual IO with 4-Byte Address	BCH	CA15-8 / 2	CA7-0 / 2	Dummy /2	Dummy / 2	Dummy/2	D7-0 / 2	D7-0 / 2	D7-0 / 2
Fast Read Quad IO	EBH	CA15-8 / 4	CA7-0 / 4	Dummy /4	Dummy / 4	D7-0 / 4	D7-0 / 4	D7-0 / 4	D7-0 / 4
Fast Read Quad IO with 4-Byte Address	ECH	CA15-8 / 4	CA7-0 / 4	Dummy /4	Dummy / 4	Dummy/4	Dummy/4	Dummy/4	D7-0 / 4
Program Load Random Data	84H	CA15-8	CA7-0	D7-0	Next byte				
Program Load	02H	CA15-8	CA7-0	D7-0	Next byte				
Program Load Random Data x4	34H	CA15-8	CA7-0	D7-0 / 4	Next byte				
Program Load x4	32H	CA15-8	CA7-0	D7-0 / 4	Next byte				
Program Execute	10H	PA23-16	PA15-8	PA7-0					
Block Erase	D8H	PA23-16	PA15-8	PA7-0					
Reset	FFH								

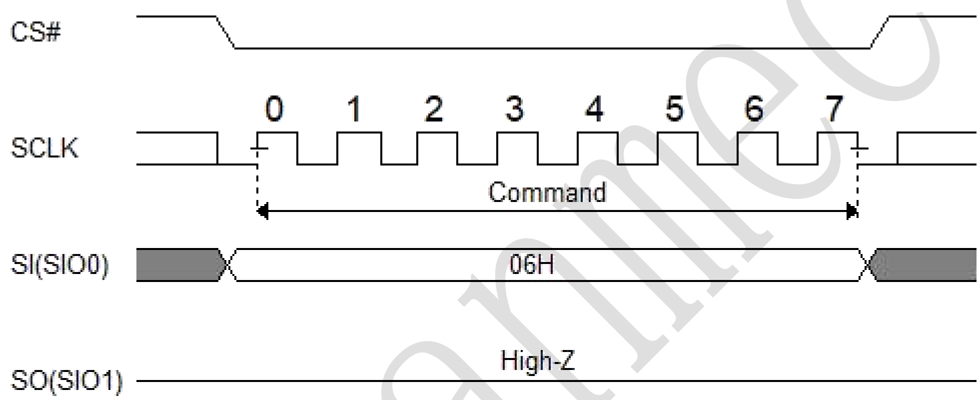
10. WRITE OPERATIONS

10.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

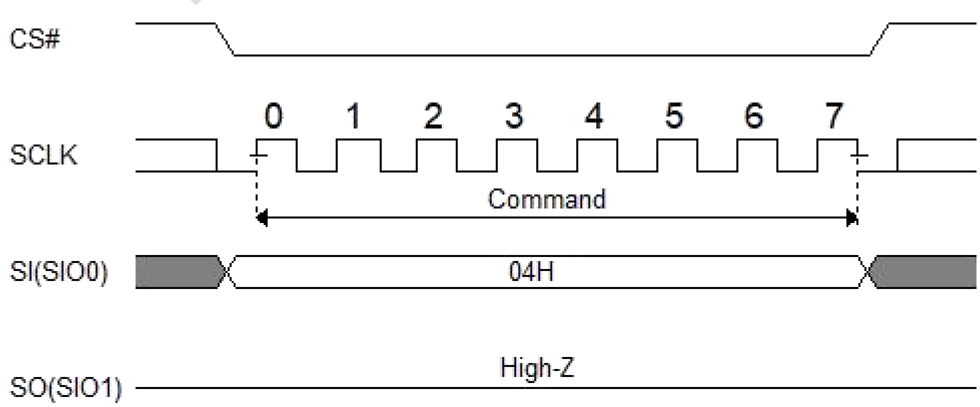
The WEL bit can be cleared after a reset command.



10.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase



11. READ OPERATIONS

11.1 Page Read

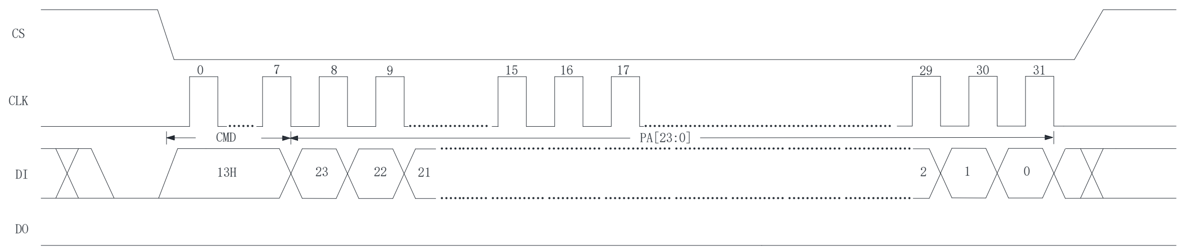
The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13H (PAGE READ to cache)
- 0FH (GET FEATURES command to read the status)
- Read from cache command to output data

The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the GET FEATURE(0FH) command can be issued to monitor the status. Followed the page read operation, the Read From Cache command must be issued in order to read out the data from cache. The output data starts at the initial address specified in the command, once it reaches the ending boundary of whole page section, the output will return FFH until CS# is pulled high to terminate this operation. Refer waveforms to view the entire READ operation.

11.2 Page Read to Cache (13H)

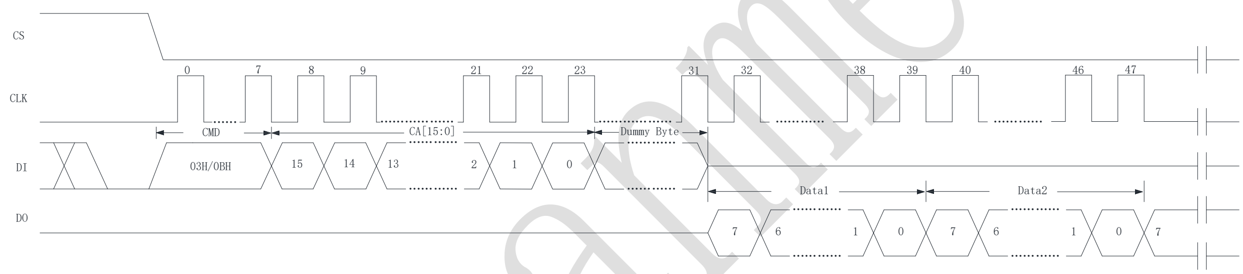
The command page read to cache is read the data from flash array to cache register.



Page Read Timing Diagram

11.3 Read (03H) or Fast Read(0BH)

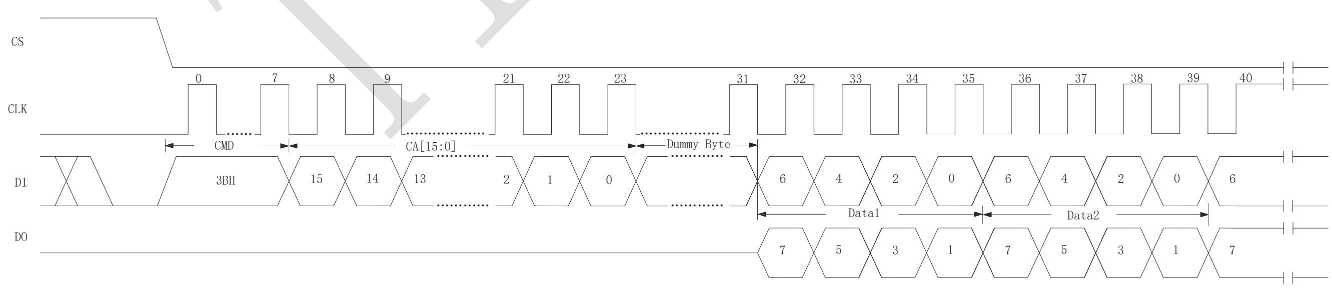
The command sequence is shown below.



Read Timing Diagram

11.4 Fast Read x2 (3BH)

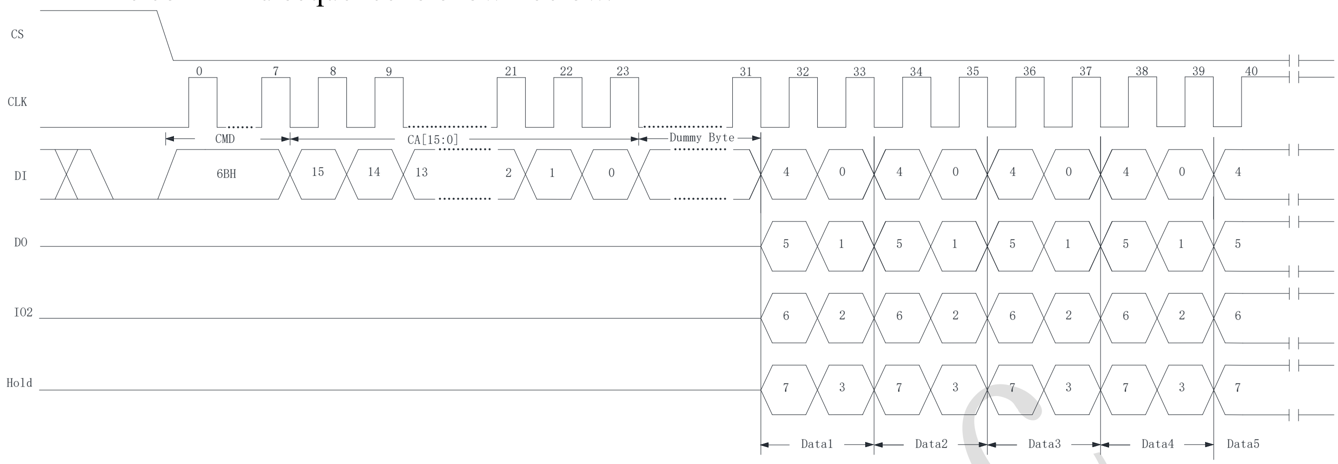
The command sequence is shown below.



Fast Read x2 Timing Diagram

11.5 Fast Read x4 (6BH)

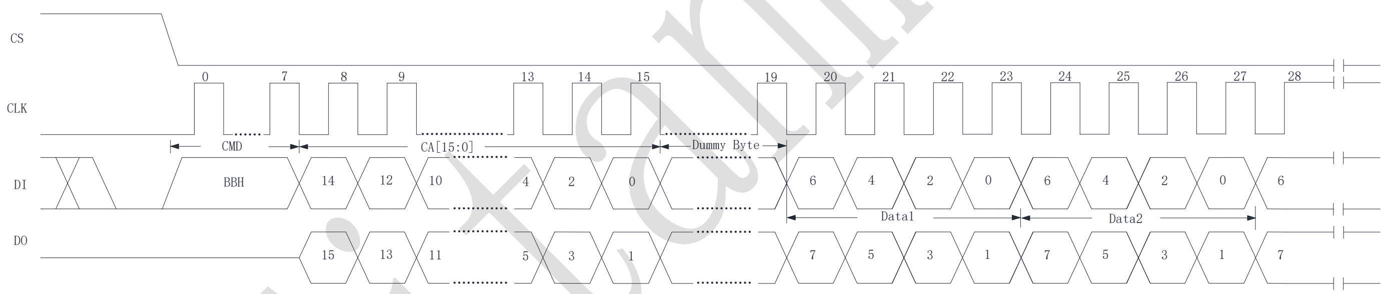
The command sequence is shown below.



Fast Read x4 Timing Diagram

11.6 Fast Read Dual IO (BBH)

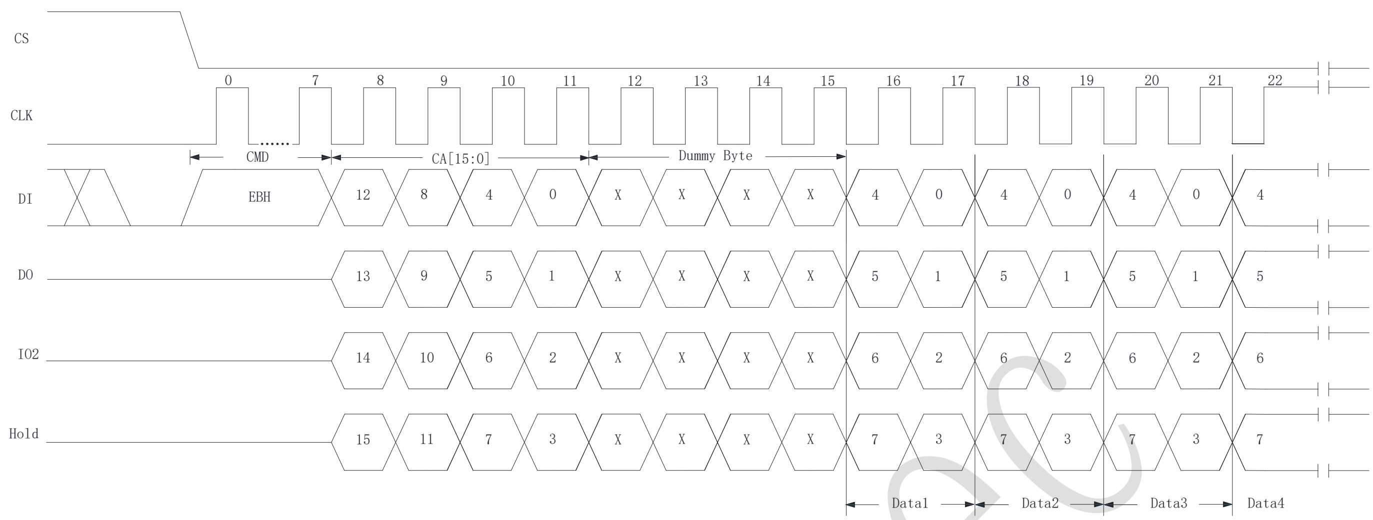
The command sequence is shown below.



Fast Read Dual IO Timing Diagram

11.7 Fast Read Quad IO (EBH)

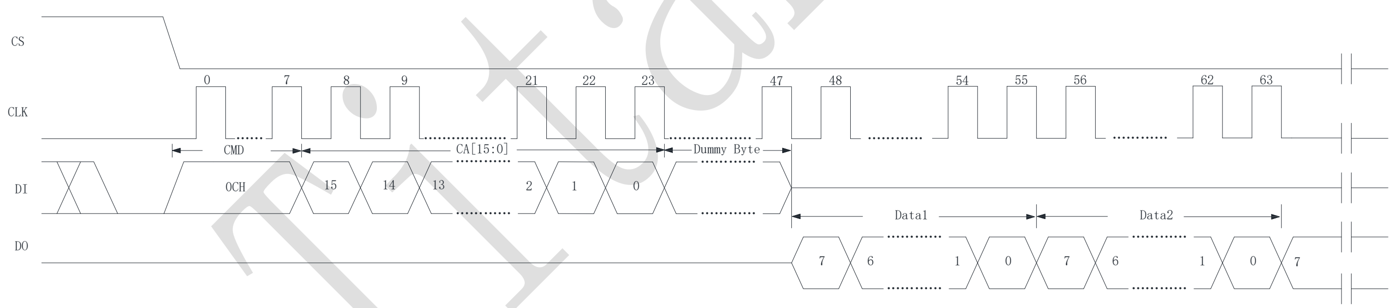
The command sequence is shown below.



Fast Read Quad IO Timing Diagram

11.8 Fast Read with 4-Byte Address(0CH)

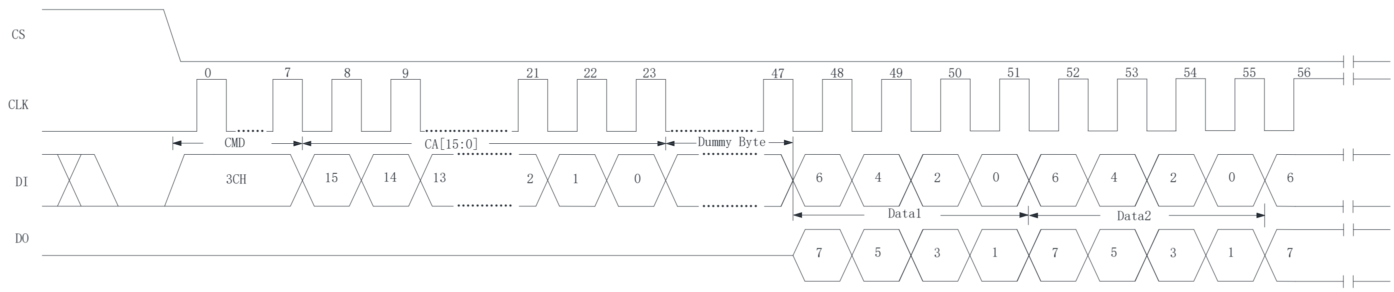
The command sequence is shown below.



Fast Read with 4-Byte Address Timing Diagram

11.9 Fast Read x 2 with 4-Byte Address (3CH)

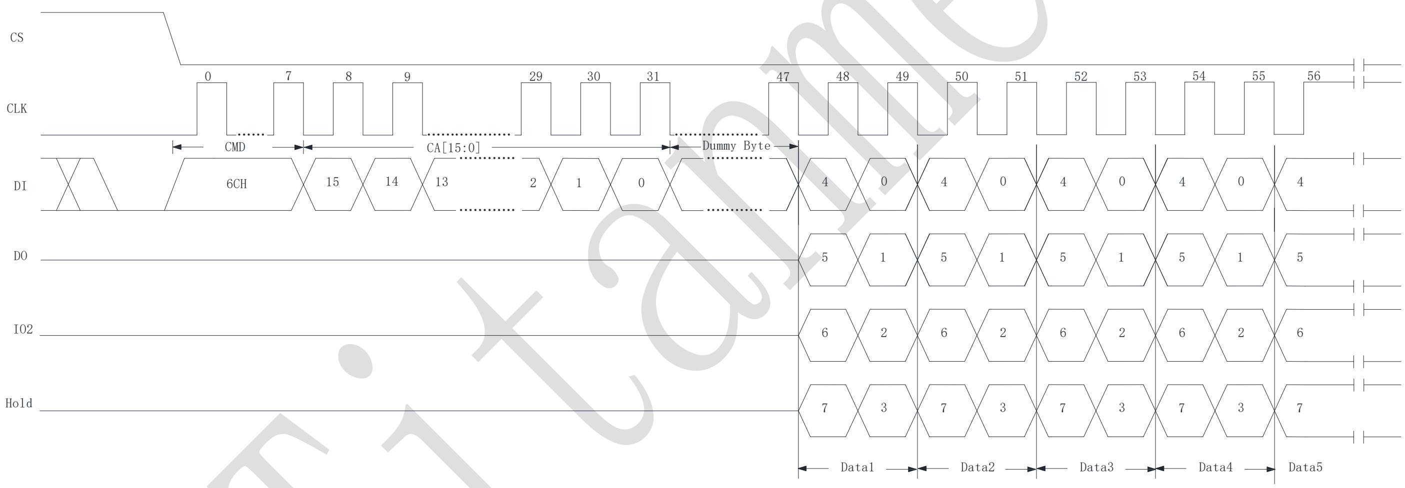
The command sequence is shown below.



Fast Read x 2 with 4-Byte Address Timing Diagram

11.10 Fast Read x 4 with 4-Byte Address (6CH)

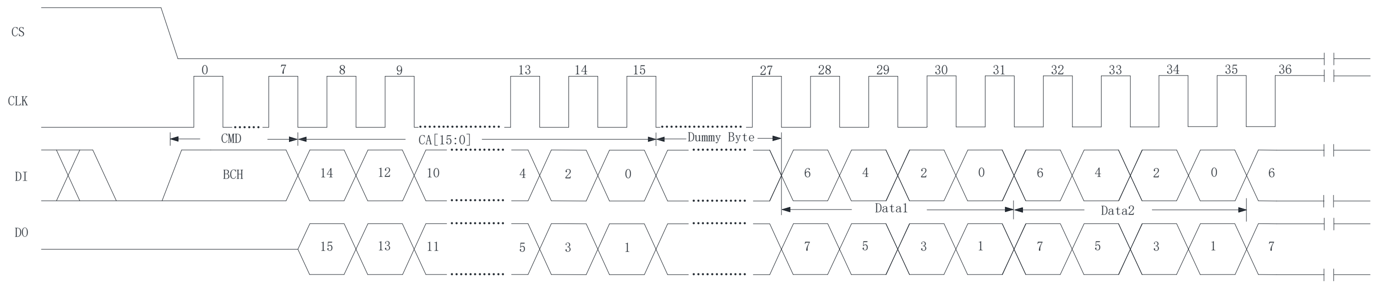
The command sequence is shown below.



Fast Read x 4 with 4-Byte Address Timing Diagram

11.11 Fast Read Dual IO with 4-Byte Address (BCH)

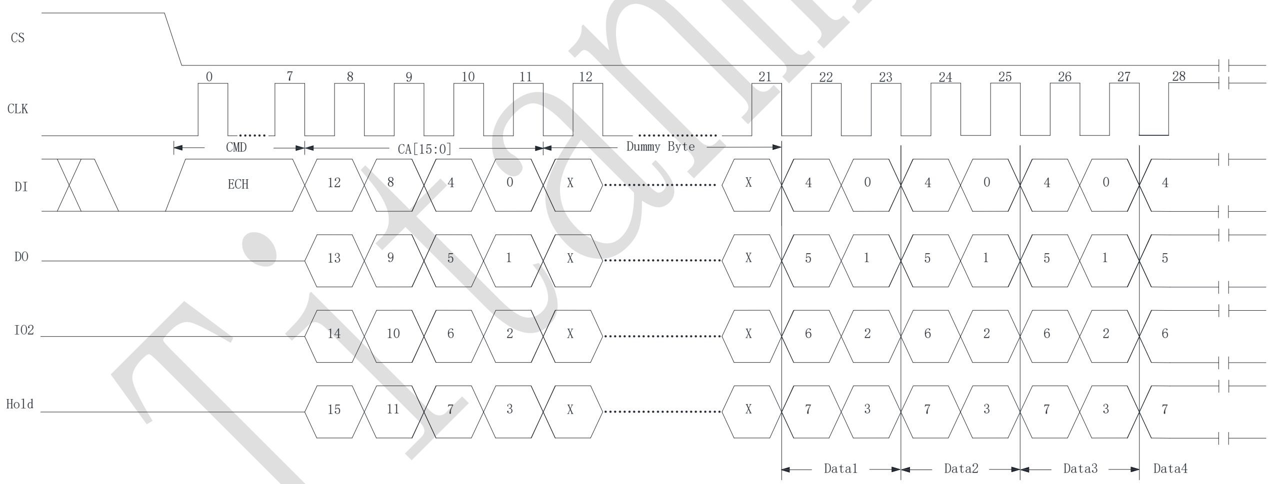
The command sequence is shown below.



Fast Read Dual IO with 4-Byte Address Diagram

11.12 Fast Read Quad IO with 4-Byte Address (ECH)

The command sequence is shown below.

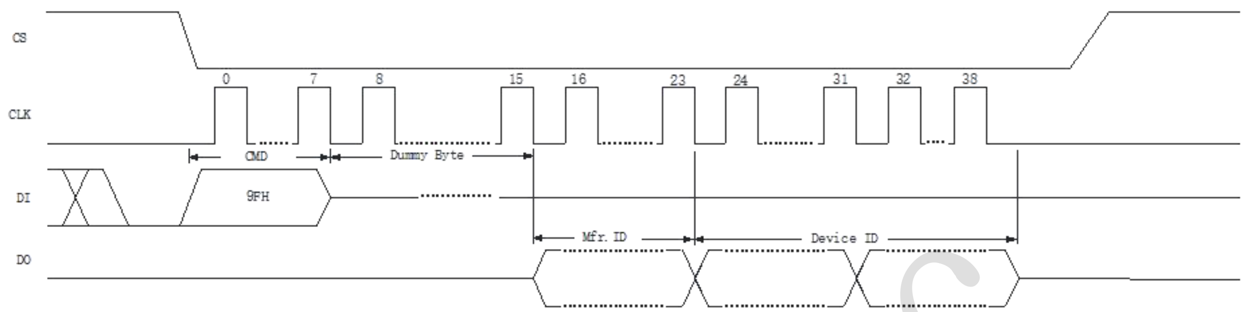


Fast Read Quad IO with 4-Byte Address Timing Diagram

11.13 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device.

The READ ID command outputs the Manufacturer ID and the device ID.



Read ID Timing Diagram

ID Table

PART NO	MID	DID15-DID0
TM1F512MUAI	3Dh	0030h
TM1F1GUAI	3Dh	0031h
TM1F2GUAI	3Dh	0032h
TM1F4GUAI	3Dh	0034h

11.14 Read UID

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement are stored by the target. For example, reading byte 32-63 returns to the host another copy of the UID and its complement.

UID Table

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 00h, read data from array to cache.
4. Use 0FH (GET FEATURES command) read the status.
5. User can use Read from cache command (03H/0BH), read 16 bytes UID from cache

11.15 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the SPI-NAND Flash configuration of a device. A minimum of three copies of the parameter page are stored in the device. The Read from Cache command can be used to change the location of data output.

Sequence is as follows:

1. Use Set Feature command to set B0 register, to enable OTP_EN.
2. Use Get Feature command to get data from B0 register and check if the OTP_EN is enable.
3. Use Page Read to Cache (13h) command with address 01h. Load parameter page from array to cache.
4. Use 0Fh (GET FEATURES command) read the status
5. User can use Read from cache command (03h/0Bh), read parameter page from cache.

12. PROGRAM OPERATIONS

12.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to whole page bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

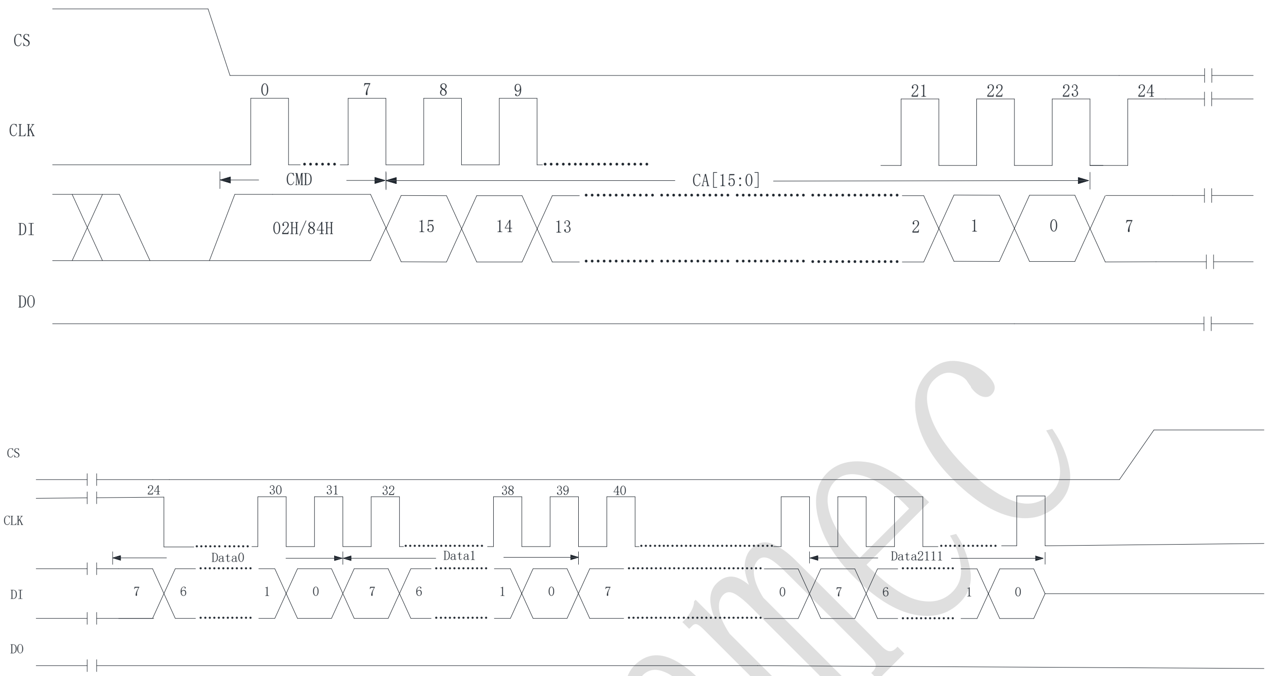
Firstly, a PROGRAM LOAD (02H/32H) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by column address, then the data bytes to be programmed. The Program address should be in sequential order in a block. The data bytes are loaded into a cache register that is whole page long. If more than one page data are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 9-1 shows the PROGRAM LOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

Note:

1. The contents of Cache Register don't reset when Program Random Load (84h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h) command, the 0xFF is output to the address that data was not loaded by Program Load (02h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h) command, the contents of Cache Register are output to the NAND array.
4. The Program address should be in sequential order in a block

12.2 Program Load (PL) (02H)/Program Load Random Data(84H)

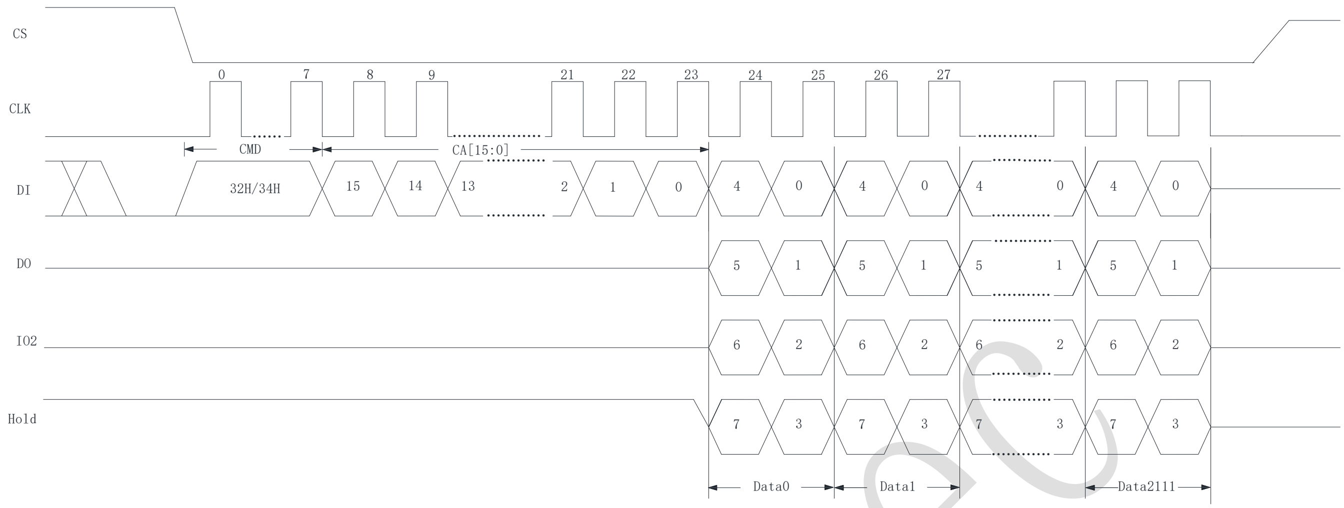
The command sequence is shown below.



Program Load/Load Random Data Timing Diagram

12.3 Program Load x4 (PL x4) (32H)/Program Load Random Data x4(34H)

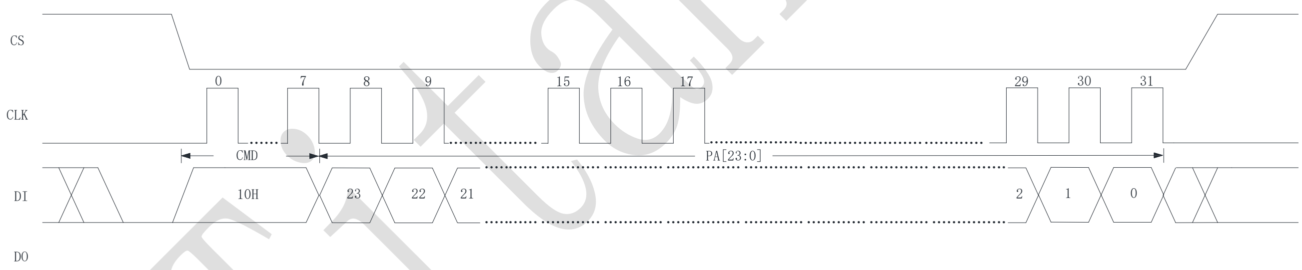
The command sequence is shown below.



Program Load/Load Random Data x4 Timing Diagram

12.4 Program Execute (PE) (10H)

The command sequence is shown below.



Program Execute Timing Diagram

13. ERASE OPERATIONS

13.1 Block Erase (D8H)

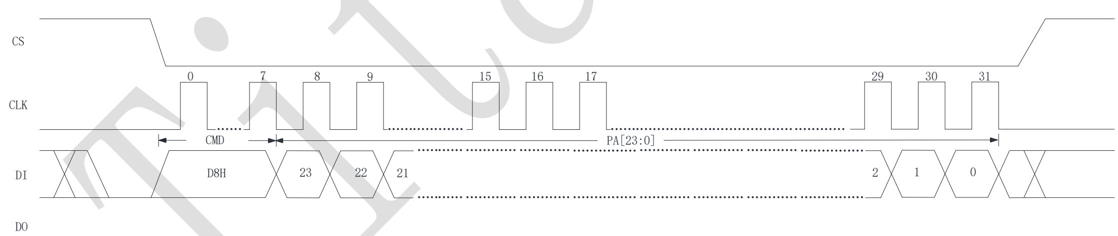
The BLOCK ERASE (D8H) command is used to erase at the block level. The BLOCK ERASE command (D8H) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

• 06H (WRITE ENBALE command)

• D8H (BLOCK ERASE command)

• 0FH (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, the WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. The WRITE ENABLE command must be followed by the BLOCK ERASE (D8H) command. This command requires 8-bit dummy clocks and the 16-bit page address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tBERS time during the BLOCK ERASE operation. The GET FEATURES (0FH) command can be used to monitor the status of the operation.

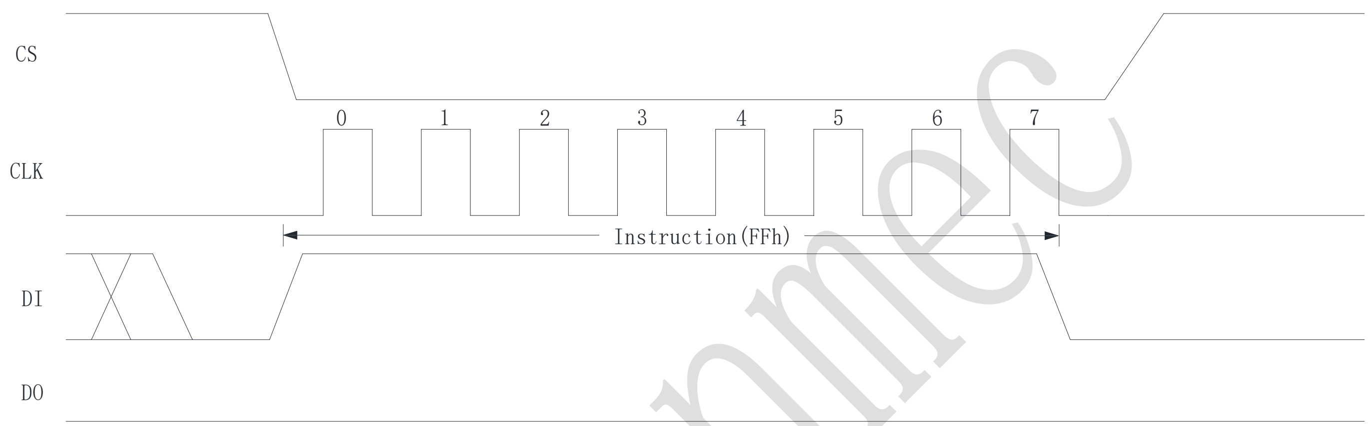


Block Erase Timing Diagram

14. RESET OPERATIONS

14.1 Reset (FFH)

The RESET (FFH) command stops all operations and the status. For example, in case of a program or erase or read operation, the reset command can make the device enter the idle state. During a cache program or cache read, a reset can also stops the previous operation and the pending operation.



Reset Timing Diagram

15. FEATURE OPERATIONS

15.1 Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Feature such as OTP can be enabled or disabled by setting specific feature bits (shown in the below table).The status registers (C0H) is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06H) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFH) command is issued.

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP-PRT	OTP-EN	Reserved	ECC-EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P-FAIL	E-FAIL	WEL	OIP

Note:

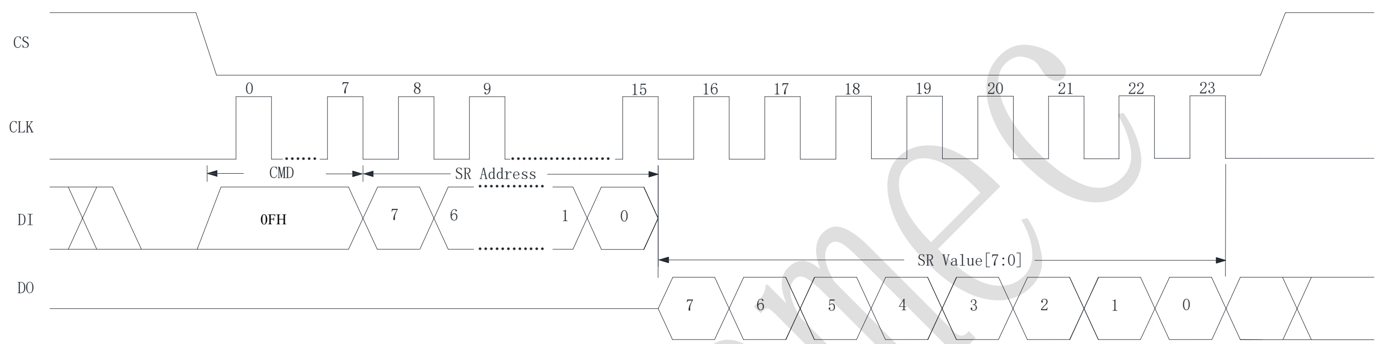
1. If QE is enabled, the quad IO operations can be executed.
2. These registers A0H/B0H are write/read type.
3. The OTP-PRT is non-volatile, others bits are volatile.
4. The Register Bit default value after power-up refers to Table Register Bit Descriptions.

Register Bit Descriptions

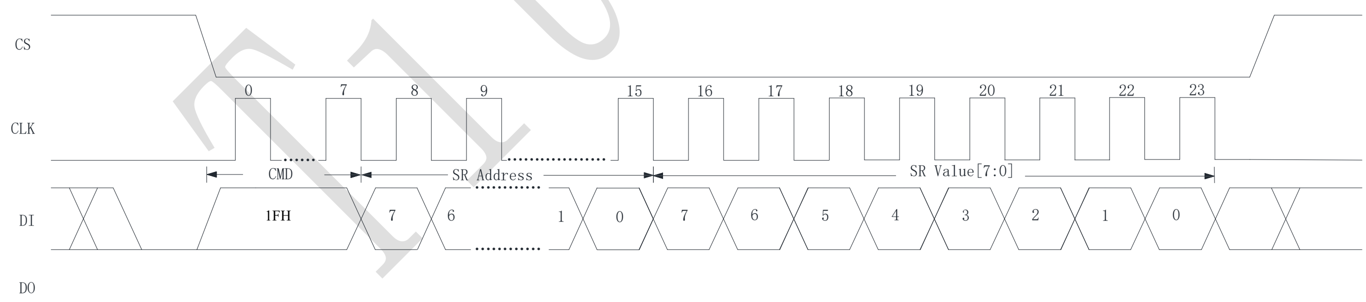
Bit	Bit Name	After Power up	After Reset command (FFH)	Description
BRWD	Block Register Write Disable	0	No Change	Which is used combined with WP#, If BRWD is high enabled and WP# is LOW, then the Protection register cannot be changed
BP2 BP1 BP0 INV CMP	Block Protection bits	1 1 1 0 0	No Change	Used combination, refer to chapter Block Protection.
OTP_PRT OTP_EN	OTP Region bits	0 0 Before OTP Set	No Change	used combination, refer to chapter OTP Region.

Bit	Bit Name	After Power up	After Reset command (FFH)	Description
ECC-EN	ECC Enable Latch	1	No Change	The device offers data corruption protection by offering internal ECC.READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC-EN.ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the "active" state when ECC enable.
QE	The Quad Enable bit	1	No Change	This bit indicates that whether the quad IO operations can be executed. If QE is set to 1, the quad IO operations can be executed
ECC-S0 ECC-S1	ECC Status	0 0	0 0	ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-S1, ECC-S0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-EN=0. These bits will be cleared to 0 after a power cycle or a RESET command.
P_FAIL E_FAIL	Program/Erase Failure	0 0	0 0	The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory array or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device RESET instruction.
WEL	Write Enable Latch	0	0	Write Enable Latch (WEL) is a read only bit in the status register that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read, Program Execute and Bad Block Management for OTP pages.
OIP	Operation In Progress	0	0	OIP is a read only bit in the status register that is set to a 1 state when the device is powering up or executing a Page Data Read, Bad Block Management, Program Execute, Block Erase, Program Execute for OTP area, OTP Locking or after a Continuous Read instruction. During this time the device will ignore further

Bit	Bit Name	After Power up	After Reset command (FFH)	Description
				instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the OIP bit will be cleared to a 0 state indicating the device is ready for further instructions.



Get Features Timing Diagram



Set Features Timing Diagram

15.2 Status Register

The NAND Flash device has status registers (C0H) that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH) command, followed by the feature address C0H (see FEATURE OPERATION).

ECC-1	ECC-0	Description
0	0	No bit errors were detected during the previous read algorithm
0	1	Bit errors (<8) were detected and corrected
1	1	Bit errors (=8) were detected and corrected.
1	0	Bit errors greater than ECC capability(>8 bits) and not corrected

15.3 OTP Region

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 10 full pages are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0. To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, pages 02h–0Bh can be programmed in sequential order by PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands (when not yet protected), and read out by PAGE READ (13h) command and output data by READ from CACHE (03h/0Bh/3Bh/6Bh/BBh/EBh). When ECC is enabled, data written in the OTP area is ECC protected.

OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region, read and program data
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10h) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

Access to OTP data

- Issue the SET FEATURES command (1Fh)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0Fh command.

- Issue the SET FEATURES command (1Fh)
- Set feature bit OTP_EN and OTP_PRT
- 06h (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10h) command.

15.4 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the "locked" state, i.e., feature bits BP0, BP1and BP2 are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0. When an ERASE command is issued to a locked block, the erase failure, status bit E_FAIL set to 1. When a PROGRAM command is issued to a locked block, program failure, status bit P_FAIL set to 1.

To enable the Write Protection (WP#), the Quad Enable bit (QE) of feature (B0[0]) must be set to 0.

Block Lock Register Block Protect Bits

TM1F1GUAI						
CMP	**INV**	**BP2**	**BP1**	**BP0**	**PROTECTEDPAGE ADDRESS PA[15:0]**	**PROTECTED PORTION**
X	X	0	0	0	NONE	None—all unlocked
0	0	0	0	1	FC00h～FFFFh	Upper 1/64 locked
0	0	0	1	0	F800h～FFFFh	Upper 1/32 locked
0	0	0	1	1	F000h - FFFFh	Upper 1/16 locked
0	0	1	0	0	E000h～FFFFh	Upper 1/8 locked
0	0	1	0	1	C000h - FFFFh	Upper 1/4 locked
0	0	1	1	0	8000h - FFFFh	Upper 1/2 locked
X	X	1	1	1	0000h～FFFFh	All locked (default)
0	1	0	0	0	0000h～03FFh	Lower 1/64 locked
0	1	0	1	0	0000h～07FFh	Lower 1/32locked
0	1	0	1	1	0000h～0FFFh	Lower 1/16 locked
0	1	1	0	0	0000h～1FFFh	Lower 1/8 locked
0	1	1	0	1	0000h～3FFFh	Lower 1/4 locked
0	1	1	1	0	0000h～7FFFh	Lower 1/2 locked
1	0	0	0	1	0000h～FBFFh	Lower 63/64 locked
1	0	0	1	0	0000h～F7FFh	Lower31/32 locked
1	0	0	1	1	0000h～EFFFh	Lower 15/16 locked
1	0	1	0	0	0000h～DFFFh	Lower7/8 locked
1	0	1	0	1	0000h～BFFFh	Lower3/4 locked
1	0	1	1	0	0000h～003FH	Block0
1	1	0	0	1	0400h～FFFFh	Upper 63/64 locked
1	1	0	1	0	0800h～FFFFh	Upper31/32 locked
1	1	0	1	1	1000h～FFFFh	Upper 15/16 locked
1	1	1	0	0	2000h～FFFFh	Upper7/8 locked
1	1	1	0	1	4000h～FFFFh	Upper3/4 locked
1	1	1	1	0	0000h～003FH	Block0

TM1F2GUAI/TM1F4GUAI						
CMP	**INV**	**BP2**	**BP1**	**BP0**	**PROTECTEDPAGE ADDRESS PA[15:0]**	**PROTECTED PORTION**
X	X	0	0	0	NONE	None—all unlocked
0	0	0	0	1	1F800h～1FFFFh	Upper 1/64 locked
0	0	0	1	0	1F000h～1FFFFh	Upper 1/32 locked
0	0	0	1	1	1E000h -1FFFFh	Upper 1/16 locked
0	0	1	0	0	1C000h～1FFFFh	Upper 1/8 locked
0	0	1	0	1	18000h - 1FFFFh	Upper 1/4 locked
0	0	1	1	0	10000h - 1FFFFh	Upper 1/2 locked
X	X	1	1	1	00000h～1FFFFh	All locked (default)
0	1	0	0	0	00000h～007FFh	Lower 1/64 locked
0	1	0	1	0	00000h～00FFFh	Lower 1/32locked
0	1	0	1	1	00000h～01FFFh	Lower 1/16 locked
0	1	1	0	0	00000h～03FFFh	Lower 1/8 locked
0	1	1	0	1	00000h～07FFFh	Lower 1/4 locked
0	1	1	1	0	00000h～0FFFFh	Lower 1/2 locked
1	0	0	0	1	00000h～1F7FFh	Lower 63/64 locked
1	0	0	1	0	00000h～1EFFFh	Lower31/32 locked
1	0	0	1	1	00000h～1DFFFh	Lower 15/16 locked
1	0	1	0	0	00000h～1BFFFh	Lower7/8 locked
1	0	1	0	1	00000h～17FFFh	Lower3/4 locked
1	0	1	1	0	00000h～0003FH	Block0
1	1	0	0	1	00800h～1FFFFh	Upper 63/64 locked
1	1	0	1	0	01000h～1FFFFh	Upper31/32 locked
1	1	0	1	1	02000h～1FFFFh	Upper 15/16 locked
1	1	1	0	0	04000h～1FFFFh	Upper7/8 locked
1	1	1	0	1	08000h～1FFFFh	Upper3/4 locked
1	1	1	1	0	00000h～0003FH	Block0

When WP# is not LOW, user can issue bellows commands to alter the protection states as want.

- Issue SET FEATURES register write (1Fh)
- Issue the feature bit address (A0h) and the feature bits combination as the table

15.5 Internal ECC

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled by default when device powered on, so the default READ and PROGRAM commands operate with internal ECC in the "active" state when ECC enable.

To enable/disable ECC, perform the following command sequence:

• Issue the SET FEATURES command (1FH) to set the feature bit ECC_EN:

1. To enable ECC, Set ECC_EN to 1.
2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected (error bits≤8 bits), the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.The ECC protection format as follow:

• all data in main area and spare areas data are protected.

The Distribution of ECC Segment and Spare Area in a Page（2KB+128B）

<table>
<tr><td colspan="8">Main Area(2KB)</td></tr>
<tr><td colspan="8">User data</td></tr>
<tr><td colspan="2">Main0</td><td colspan="2">Main1</td><td colspan="2">Main2</td><td colspan="2">Main3</td></tr>
<tr><td colspan="2">512B</td><td colspan="2">512B</td><td colspan="2">512B</td><td colspan="2">512B</td></tr>
<tr><td colspan="2">Sector0</td><td colspan="2">Sector1</td><td colspan="2">Sector2</td><td colspan="2">Sector3</td></tr>
<tr><td colspan="8">Spare Area(128B)</td></tr>
<tr><td colspan="4">User meta data</td><td colspan="4">ECC Parity Data</td></tr>
<tr><td>Spare0</td><td>Spare1</td><td>Spare2</td><td>Spare3</td><td>Spare0</td><td>Spare1</td><td>Spare2</td><td>Spare3</td></tr>
<tr><td>16B</td><td>16B</td><td>16B</td><td>16B</td><td colspan="4">64B</td></tr>
</table>

ECC Protect and Spare Area（2KB+128B）

Min Byte Address	Max Byte Address	ECC Protected	Area	Description
000h	1FFh	Yes	Main0	User data 0
200h	3FFh	Yes	Main1	User data 1
400h	5FFh	Yes	Main2	User data 2
600h	7FFh	Yes	Main3	User data 3
800h[1]	80Fh	Yes	Spare 0	User meta data 0
810h	81Fh	Yes	Spare 1	User meta data 1
820h	82Fh	Yes	Spare 2	User meta data 2
830h	83Fh	Yes	Spare 3	User meta data 3
840h	87Fh	Yes	Spare area	Inter ECC parity data[2]

Note:

(1) 800h is reserved for initial bad block mark.

(2) The ECC for main/spare area(840h-87Fh) is prohibited for user.

The Distribution of ECC Segment and Spare Area in a Page（4KB+256B）

<table>
<tr><td colspan="8">Main Area(4KB)</td></tr>
<tr><td colspan="8">User data</td></tr>
<tr><td>Main0</td><td>Main1</td><td>Main2</td><td>Main3</td><td>Main4</td><td>Main5</td><td>Main6</td><td>Main7</td></tr>
<tr><td>512B</td><td>512B</td><td>512B</td><td>512B</td><td>512B</td><td>512B</td><td>512B</td><td>512B</td></tr>
<tr><td>Sector0</td><td>Sector1</td><td>Sector2</td><td>Sector3</td><td>Sector4</td><td>Sector5</td><td>Sector6</td><td>Sector7</td></tr>
</table>

<table>
<tr><td colspan="9">Spare Area(256B)</td></tr>
<tr><td colspan="8">User meta data</td><td>ECC Parity Data</td></tr>
<tr><td>Spare0</td><td>Spare1</td><td>Spare2</td><td>Spare3</td><td>Spare4</td><td>Spare5</td><td>Spare6</td><td>Spare7</td><td rowspan="2">128B</td></tr>
<tr><td>16B</td><td>16B</td><td>16B</td><td>16B</td><td>16B</td><td>16B</td><td>16B</td><td>16B</td></tr>
</table>

ECC Protect and Spare Area（4KB+256B）

Min Byte Address	Max Byte Address	ECC Protected	Area	Description
0000h	01FFh	Yes	Main0	User data 0
0200h	03FFh	Yes	Main1	User data 1
0400h	05FFh	Yes	Main2	User data 2
0600h	07FFh	Yes	Main3	User data 3
0800h	09FFh	Yes	Main4	User data 4
0A00h	0BFFh	Yes	Main5	User data 5
0C00h	0DFFh	Yes	Main6	User data 6
0E00h	0FFFh	Yes	Main7	User data 7
1000h(1)	100Fh	Yes	Spare 0	User meta data 0
1010h	101Fh	Yes	Spare 1	User meta data 1
1020h	102Fh	Yes	Spare 2	User meta data 2
1030h	103Fh	Yes	Spare 3	User meta data 3
1040h	104Fh	Yes	Spare 4	User meta data 4
1050h	105Fh	Yes	Spare 5	User meta data 5
1060h	106Fh	Yes	Spare 6	User meta data 6
1070h	107Fh	Yes	Spare 7	User meta data 7
1080h	10FFh	Yes	Spare area	Inter ECC parity data(2)

Note:

(1) 1000h is reserved for initial bad block mark.

(2) The ECC for main/spare area(1080h-10FFh) is prohibited for user.

16. Block Management

16.1 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (NVB) of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad- block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFH data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

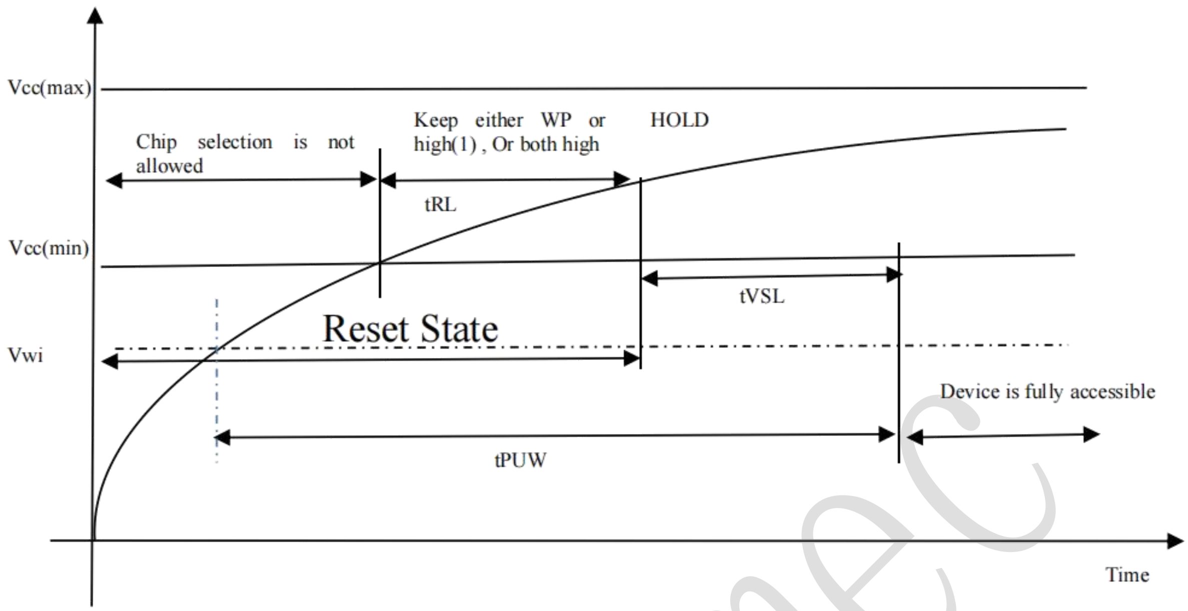
Bad Block Mark information

TM1F1GUAI	
Description	Requirement
Minimum number of valid blocks (NVB)	1004
Total available blocks per die	1024
First spare area location	Byte 2048
Bad-block mark	00h(use non FFH to check)

TM1F2GUAI	
Description	Requirement
Minimum number of valid blocks (NVB)	2008
Total available blocks per die	2048
First spare area location	Byte 2048
Bad-block mark	00h(use non FFH to check)

TM1F4GUAI	
Description	Requirement
Minimum number of valid blocks (NVB)	2008
Total available blocks per die	2048
First spare area location	Byte 4096
Bad-block mark	00h(use non FFH to check)

17. POWER ON TIMING



Power on Timing Sequence

Power-On Timing and Write Inhibit Threshold for 3.3V

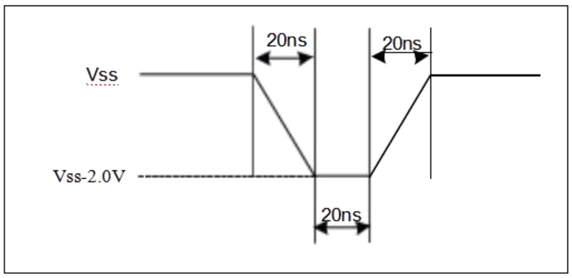
Symbol	Parameter	Min	Max	Unit
Vcc(min)		2.7		V
Vcc(max)			3.6	V
VWI	Write Inhibit Voltage		2.5	V
tRL(1)	Time of keeping either WP or HOLD high, Or both high	800		us
tVSL	Vcc(min) To CS# Low	1.5	2	ms
tPUW	Time Delay From VCC(WI) To Write Instruction	2.5		ms

Note:

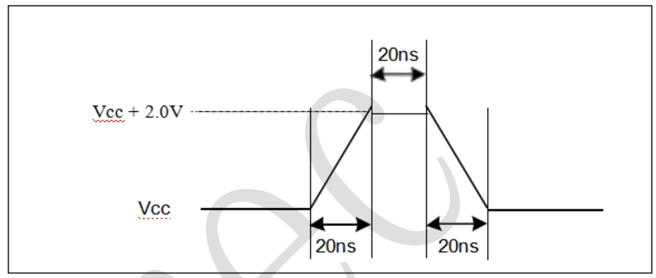
(1) After Vcc reach Vcc(min), to release reset state, host should keep either WP or HOLD high for the time of tRL at last. Or reset command(FFH) can also release reset state.

18. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 105	℃
Storage Temperature	-65 to 150	℃
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
VCC(3.3V)	-0.6 to 4.0	V



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

19. CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Input Test Waveform and Measurement Level

20. DC CHARACTERISTIC

(T= -40℃~85℃/-40℃~105℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current (CMOS) for 45℃	CS#=VCC, V_{IN}=VCC or VSS		65		μA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O)			30	mA
I_{CC3}	Operating Current (Program)				30	mA
I_{CC4}	Operating Current (Erase)				30	mA
I_{CC5}	Deep power-down Current			35		
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

Note:
Value guaranteed by design and/or characterization, not 100% tested in production.

21. AC CHARACTERISTICS

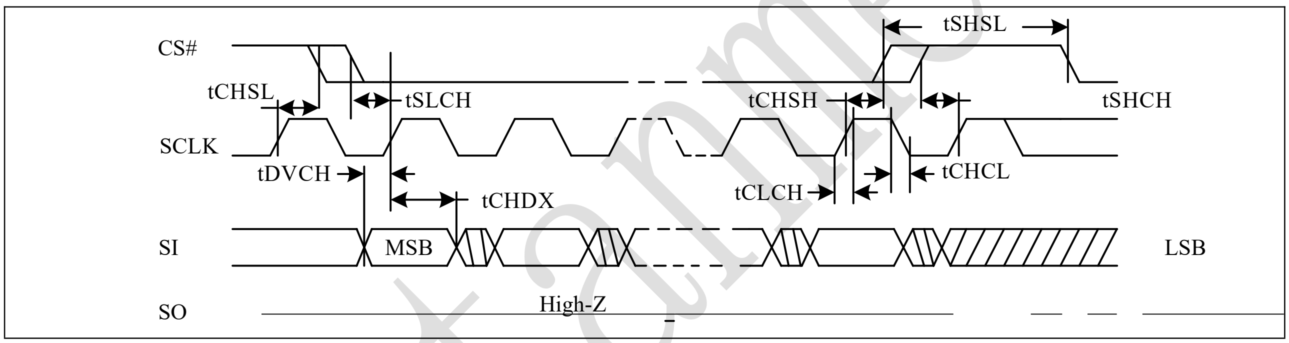
(T= -40℃~85℃/-40℃~105℃, VCC=2.7~3.6V, C_L=30pF)

Symbol	Parameter	3.3V		Unit.
		Min.	Max.	
FC1	Serial Clock Frequency		104	MHz
tCH	Serial Clock High Time	4		ns
tCL	Serial Clock Low Time	4		ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2		V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2		V/ns
tCHSH	CS# Active Hold Time	5		ns
tSHCH	CS# Not Active Setup Time	5		ns
tSLCH	CS# Active Setup Time	5		ns
tCHSL	CS# Not Active Hold Time	5		ns
tSHSL/tCS	CS# High Time	20		ns
tSHQZ	Output Disable Time		20	ns
tCLQX	Output Hold Time	2		ns
tDVCH	Data In Setup Time	2		ns
tCHDX	Data In Hold Time	2		ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5		ns
tHHCH	Hold# High Setup Time (relative to Clock)	5		ns
tCHHL	Hold# High Hold Time (relative to Clock)	5		ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5		ns
tHLQZ	Hold# Low To High-Z Output		15	ns
tHHQX	Hold# High To Low-Z Output		15	ns
tCLQV	Clock Low To Output Valid		9	ns
tWHSL	WP# Setup Time Before CS# Low	20		ns
tSHWL	WP# Hold Time After CS# High	100		ns
tHODLY	Clock High To Output Valid When HSOD=1	2	7	ns

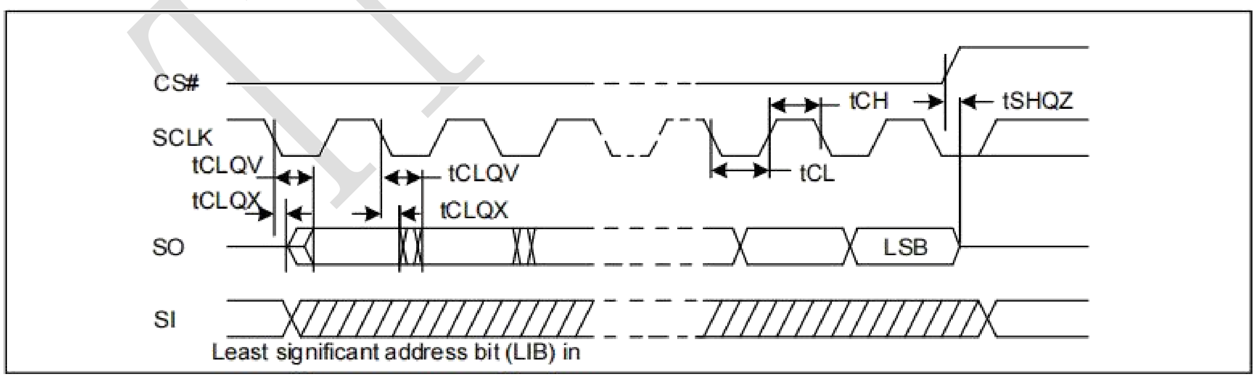
Note:
1. Value guaranteed by design and/or characterization, not 100% tested in production.

22. PERFORMANCE AND TIMING

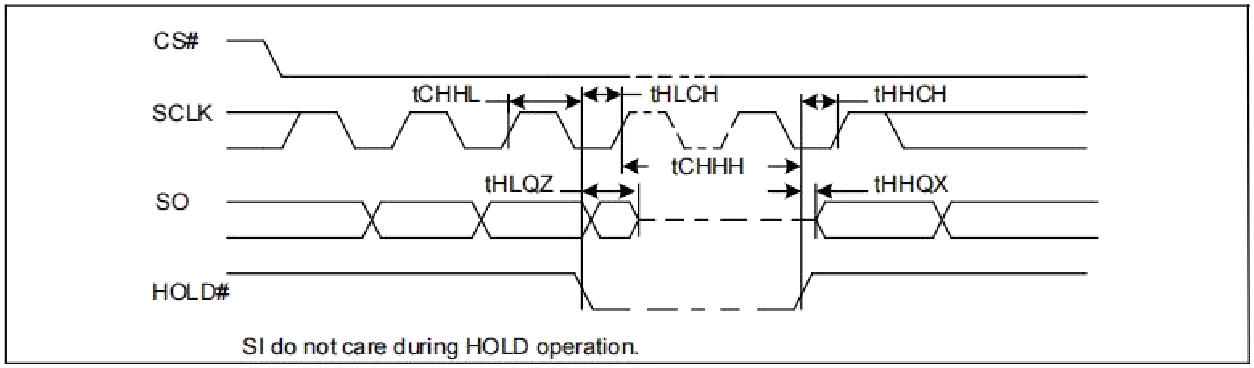
Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRST	CS# High To Next Command After Reset(FFh)			500	us
tRD	Read From Array			380	us
tRD_ECC	Read From Array with ECC		380		us
tPROG	Page Programming Time		600		us
tPROG_ECC	Page Programming Time with ECC		400	600	us
tBERS	Block Erase Time		3	5	ms
tPCBSY	Cache busy time for cache Program		20		us
tRCBSY	Cache busy time for cache Read		20		us



Serial Input Timing

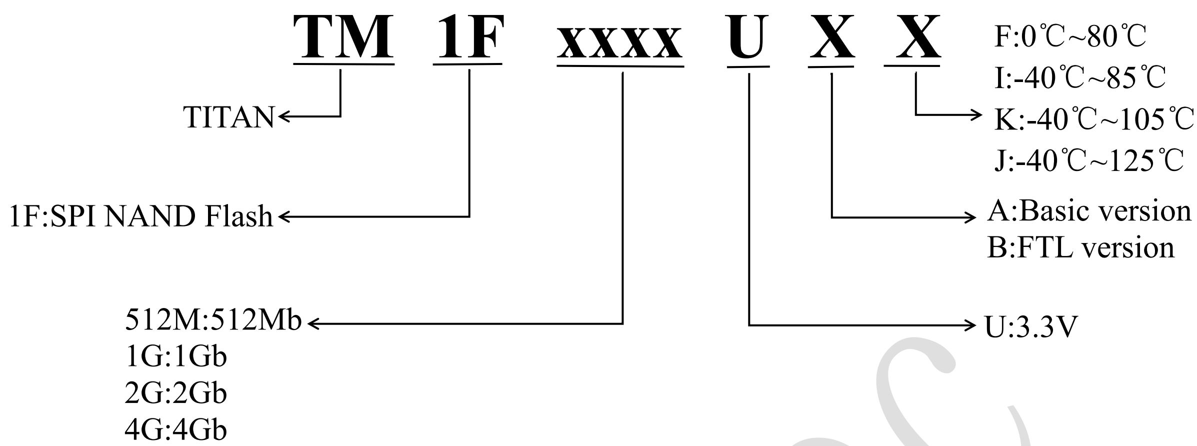


Serial Output Timing


CS#
SCLK
SO
HOLD#
tCHHL
tHLCH
tHHCH
tCHHH
tHLQZ
tHHQX
SI do not care during HOLD operation.

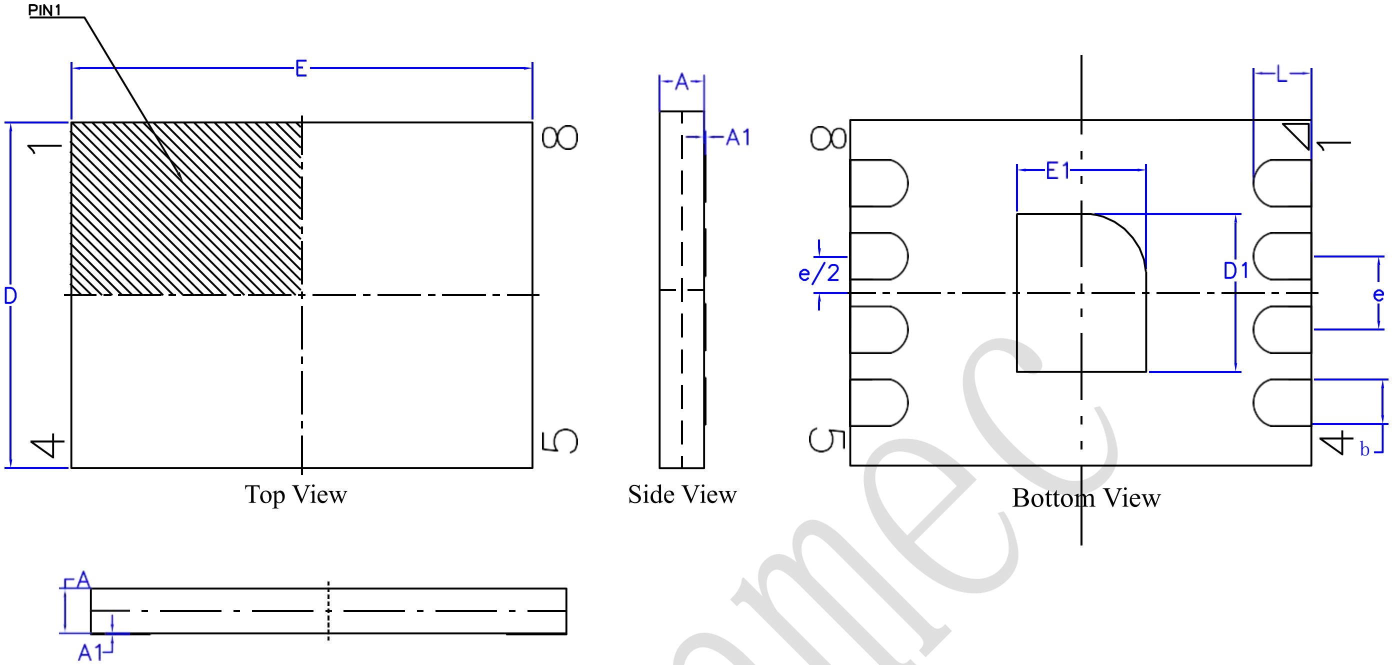
Hold Timing

23. Part Information



24. Package

LGA-8LD-6x8



Dimensions

Item	E	D	D1	E1	A	A1	b	L	e
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm
Spec	8.10 (8.00) 7.90	6.10 (6.00) 5.90	2.70	2.25	0.80 (0.75) 0.70	0.05 (0.02) 0.00	0.85 (0.80) 0.75	1.05 (1.00) 0.95	1.27BSC

Notes
1. All Dimensions are in Millimeters.
2. Dimensions Do Not include Burrs, Mold Flash, and Tie-bar Extrusions.
3. Dimension(FT) Does Not include Plating Thickness.