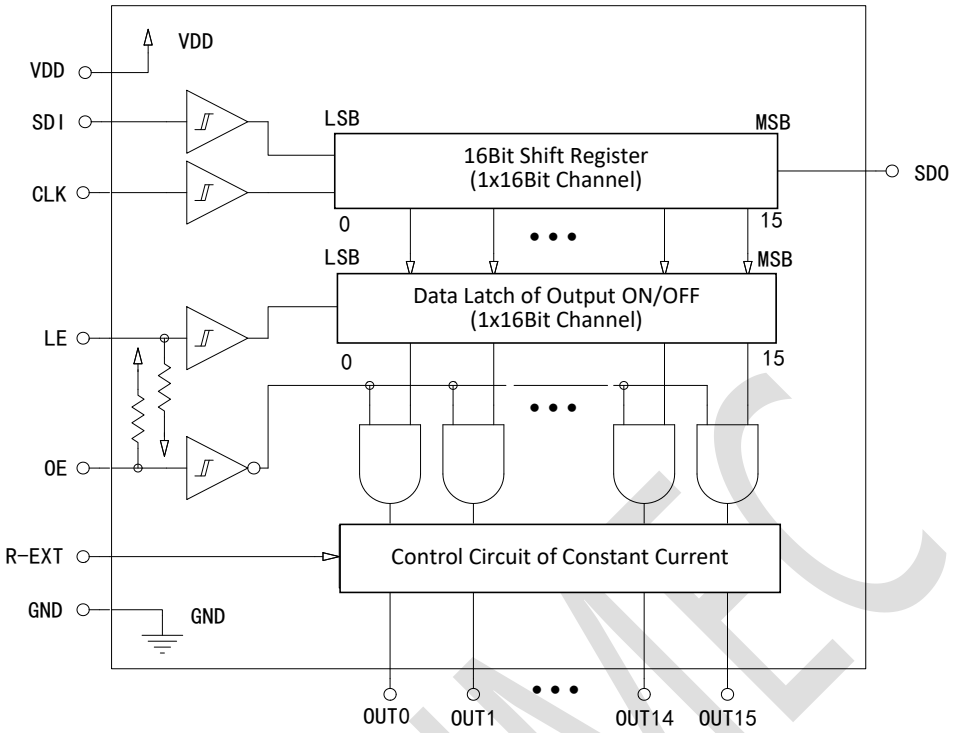
1. Features Description

TM5020C Is the driver IC designed by LED display panel. It has built-in CMOS displacement register and lock memory function. Its core integrates the displacement register and lock memory mechanism of CMOS technology, realizing the efficient conversion from serial data input to parallel data output. The chip has 16 current sources built in, and each output port stably provides a current between 3 and 36 ma to drive the LED element. These output ports support a parallel configuration to increase the output current, and their performance is highly stable to environmental changes, ensuring the accuracy of the current output. In addition, TM5020C is also designed to have a flexible current regulation function, through the external resistance of different resistance values (REXT), the user can accurately adjust the current intensity of each output port, so as to achieve careful control of LED light emitting brightness. This product has excellent performance and reliable quality.

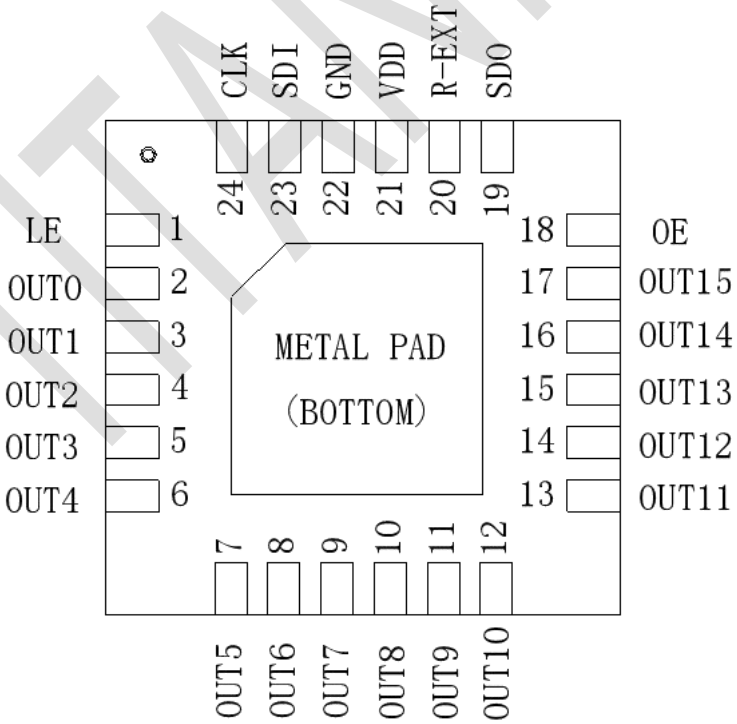
2. Functionalities and Features

- 16 output channels with constant current
- Withstand voltage of OUT port guaranteed to be 11V
- Current stability: constant current output is stable, small brightness fluctuation
- Constant current range:
  3~36mA@VDD=5V
  3~20mA@VDD=3.3V
- Precise current output value
  (between channels) max inaccuracy: ≤±2.0％
  (between chips) max inaccuracy: ≤±3.0％
- Flexible current regulation: 16 OUT current output by adjusting external resistance
- Quick response capability: minimum pulse width = 35 nS
- High-speed data transmission: up to 25 MHz data transmission rate
- Stable input characteristics: integrate the Schmidt trigger to improve the signal stability and anti-interference ability
- Wide working voltage range: 3.3V~5V
- Widely used scenarios: indoor, external single, double, full-color (dynamic, static) LED display, lighting, energy-saving lighting, etc.
- Package: QFN24

3. Internal Structure Diagram



4. PIN Diagram



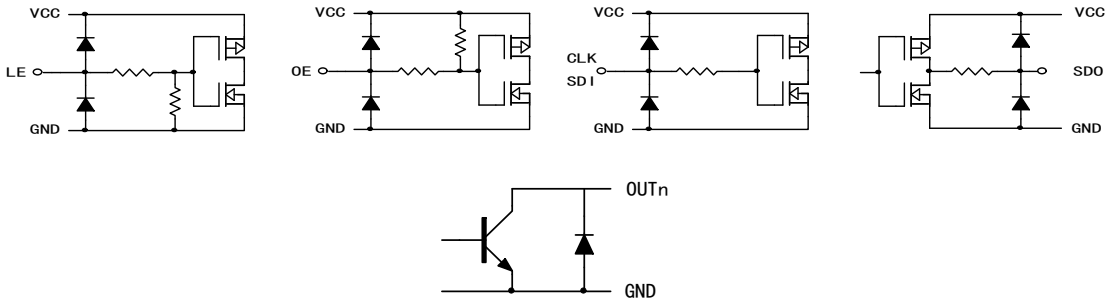
QFN24

NOTE: Metal pad is not connected to GND internally. The metal pad must be connected to GND with the printed circuit board (PCB) pattern.

5. PIN Definitions

PIN Name	PIN No.	I/O	Definition Description
SDI	23	I	Serial data input, Schmitt buffer input.
CLK	24	I	Serial data shift clock input, Schmitt buffer input, shift data on clock rise.
LE	1	I	Data latch control, Schmitt buffer input. When LE is high, serial data will be transferred to the input latch; when LE is low, data will be latched.
OE	18	I	Output enable control. When OE is low level, it will enable OUT0~OUT15 output; when OE is high level, OUT0~OUT15 output will be disabled. This pin has a built-in pull-up resistor to VDD.
R-EXT	20	I/O	Constant current value setting. It sets the current of OUT0~OUT15 output terminal, and connects an external resistor to GND.
SDO	19	O	Serial data output. It outputs on the rising edge of CLK, and can be connected to the SDI port of the next chip.
OUT0	2	O	Constant current source output. Each output can be shorted to improve the constant current.
OUT1	3	O	Constant current source output
OUT2	4	O	Constant current source output
OUT3	5	O	Constant current source output
OUT4	6	O	Constant current source output
OUT5	7	O	Constant current source output
OUT6	8	O	Constant current source output
OUT7	9	O	Constant current source output
OUT8	10	O	Constant current source output
OUT9	11	O	Constant current source output
OUT10	12	O	Constant current source output
OUT11	13	O	Constant current source output
OUT12	14	O	Constant current source output
OUT13	15	O	Constant current source output
OUT14	16	O	Constant current source output
OUT15	17	O	Constant current source output
VDD	21	-	Chip power
GND	22	-	Control logic and drive current return to ground

6. Equivalent Circuits of Input and Output



In the dry seasons or environment, it is easy to generate a lot of static electricity. Electrostatic discharge may damage the integrated circuit. Tianwei Electronics recommends taking all appropriate measures to protect the integrated circuit. Improper operations and welding may cause ESD damage or performance drops, so that the chip would work properly.

7. Absolute Maximum Rated Value Range (1)(2)

Argument Name	Argument Symbol	Limit	Unit
Power Voltage	Vdd	0～7.0	V
Input Voltage Range	Vin	-0.2～VDD+0.2V	V
Output Current (DC)	Iout	36	mA
Output Voltage Ranage	Vout	-0.2～+11.0	V
Total Current to Ground	I_{GND}	510	mA
Clock Frequency	Fclk	25	MHZ
Working Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃

(1) For these levels in the above table, the chip is not allowed to work at the limit value for a long time, otherwise the reliability of the device would be reduced and may cause permanent damage. Tianwei Electronics does not recommend that the chip works beyond these limit parameters under any other conditions.

(2) All voltage values are tested with respect to the network ground.

8. Electronics Features (VDD=5V)

Tested with VDD=5V and 25℃ except for other descriptions				TM5020C			Unit
Argument Name		Argument Symbol	Test Conditions	Min Value	Typ. Value	Max Value	
Power Voltage		VDD		4.5	5.0	5.5	V
Output Withstand Voltage Range		VO	OUT0~OUT15	——	——	11.0	V
Input Voltage of High Level		VIH	Ta=-40～+85℃	0.7*VDD	——	VDD	V
Input Voltage of Low Level		VIL	Ta=-40～+85℃	GND	——	0.3*VDD	V
Output Current		IOUT	Test circuit for reference DC characteristics	3.0	——	36.0	mA
		IOH	SDO=4.0V	——	4.4	——	mA
		IOL	SDO=1.0V	——	5.0	——	mA
Output Leaking Current		IOH	VDS=11.0V	——	——	0.5	uA
Output Voltage of High Level		VOH	IOH=-1.0mA	4.6	——	——	V
Output Voltage of Low Level		VOL	IOL=+1.0mA	——	——	0.4	V
Output Current 1		I_{OUT1}	VDS=1.0V REXT=6KΩ	——	2.95	——	mA
Current Offset		dI_{OUT1}	VDS=1.0V IOL=2.95mA REXT=6KΩ	——	±1.5	±2.5	%
Output Current 2		I_{OUT2}	VDS=1.0V REXT=735Ω	——	23.8	——	mA
Current Offset		dI_{OUT2}	VDS=1.0V IOL=23.8mA REXT=735Ω	——	±1.5	±2.5	%
Current Offset vs. Output Voltage		%/dVDS	Output Voltage=1.0~3.0V	——	±0.1	——	%/V
Current Offset vs. Power Voltage		%/dVDD	Power Voltage=4.5~5.5V	——	——	±1.0	%/V
Pull-up Resistor		R_{IN}(up)	OE	187	250	312	KΩ
Pull-down Resistor		R_{IN}(down)	LE	202	270	337	KΩ
Output Current of Voltage Source	OFF	IDD(off)1	REXT not connected， OUT0~OUT15=off	——	1.9	——	mA
		IDD(off)2	REXT=1250Ω， OUT0~OUT15=off	——	5.8	——	mA
		IDD(off)3	REXT=625Ω， OUT0~OUT15=off	——	9.6	——	mA
	ON	IDD(on)1	REXT=1250Ω， OUT0~OUT15=on	——	8.5	——	mA
		IDD(on)2	REXT=625Ω， OUT0~OUT15=on	——	12.3	——	mA

9. Electrical Characteristics (VDD=3.3V)

Tested with VDD=3.3V and 25℃ except for other descriptions					TM5020C			Unit
Argument Name		Argument Symbol	Test Conditions		Min Value	Typ. Value	Max Value	
Power Voltage		VDD			3.0	3.3	4.5	V
Output Withstand Voltage Range		VO	OUT0~OUT15		——	——	11.0	V
Input Voltage of High Level		VIH	Ta=-40～+85℃		0.7*VDD	——	VDD	V
Input Voltage of Low Level		VIL	Ta=-40～+85℃		GND	——	0.3*VDD	V
Output Current		IOUT	Test circuit for reference DC characteristics		3.0	——	20.0	mA
		IOH	SDO=2.6V		——	3.2	——	mA
		IOL	SDO=1.0V		——	5.4	——	mA
Output Leaking Current		IOH	VDS=11.0V		——	——	0.5	uA
Output Voltage of High Level		VOH	IOH=-1.0mA		2.9	——	——	V
Output Voltage of Low Level		VOL	IOL=+1.0mA		——	——	0.4	V
Output Current 1		I_{OUT1}	VDS=1.0V	REXT=6KΩ	——	2.95	——	mA
Current Offset		dI_{OUT1}	VDS=1.0V IOL=2.95mA	REXT=6KΩ	——	±1.5	±2.5	%
Output Current 2		I_{OUT2}	VDS=1.0V	REXT=885Ω	——	20.0	——	mA
Current Offset		dI_{OUT2}	VDS=1.0V IOL=20.0mA	REXT=885Ω	——	±1.5	±2.5	%
Current Offset vs. Output Voltage		%/dVDS	Output Voltage=1.0~3.0V		——	±0.1	——	%/V
Current Offset vs. Power Voltage		%/dVDD	Power Voltage=3.0~3.6V		——	——	±1.0	%/V
Pull-up Resistor		R_{IN}(up)	OE		187	250	312	KΩ
Pull-down Resistor		R_{IN}(down)	LE		202	270	337	KΩ
Output Current of Voltage Source	OFF	IDD(off)1	REXT not connected, OUT0~OUT15=off		——	1.7	——	mA
		IDD(off)2	REXT=1250Ω, OUT0~OUT15=off		——	5.3	——	mA
		IDD(off)3	REXT=885Ω, OUT0~OUT15=off		——	7.0	——	mA
	ON	IDD(on)1	REXT=1250Ω, OUT0~OUT15=on		——	8.0	——	mA
		IDD(on)2	REXT=885Ω, OUT0~OUT15=on		——	9.6	——	mA

10. Electronics Features (VDD=5V)

Tested with VDD=5V and 25℃ except for other descriptions				TM5020C			Unit
Argument Name		Argument Symbol	Test Conditions	Min Value	Typ. Value	Max Value	
Delay Time (From Low Level to High Level)	CLK↑ - OUT2n↑	TPLH1	VDD=5.0V VDS=1.0V VIH=VDD VIL=GND REXT=930Ω VL=VE=4.5V RL=184Ω CL=10pF	——	35	55	nS
	CLK↑ - OUT2n+1↑			——	35	55	nS
	LE↑ - OUT2n↑	TPLH2		——	35	55	nS
	LE↑ - OUT2n+1↑			——	35	55	nS
	OE↑ - OUT2n↑	TPLH3		——	35	55	nS
	OE↑ - OUT2n+1↑			——	45	65	nS
	CLK↑ - SDO↑	TPLH		——	25	40	nS
Transfer Delay Time (From Low Level to High Level)	CLK↑ - OUT2n↓	TPHL1		——	35	55	nS
	CLK↑ - OUT2n+1↓			——	35	55	nS
	LE↑ - OUT2n↓	TPHL2		——	35	55	nS
	LE↑ - OUT2n+1↓			——	35	55	nS
	OE↓ - OUT2n↓	TPHL3		——	35	55	nS
	OE↓ - OUT2n+1↓			——	45	65	nS
	CLK↑-SDO↓	TPHL		——	25	40	nS
Pulse Width	CLK	TWCLK		20	——	——	nS
	LE	TWLE		20	——	——	nS
	OE	TWOE		50	100	——	nS
LE Setup Time	LE↓– CLK↑	TSU(L)		5	——	——	nS
LE Hold Time	LE↑– CLK↑	TH(L)		30	——	——	nS
SDI Setup Time	SDI – CLK↑	TSU(D)		3	——	——	nS
SDI Hold Time	SDI – CLK↑	TH(D)		5	——	——	nS
CLK Maximum Rise Time		Tr		——	——	500	nS
CLK Maximum Fall Time		Tf		——	——	500	nS
SDO Rise Time		Tr		——	10	——	nS
SDO Fall Time		Tf		——	10	——	nS
Potential Rise Time of Current Output		Tr		——	35	——	nS
Potential Fall Time of Current Output		Tf		——	50	——	nS

1) The condition for these values is: the shortest OE under the condition that the output channel maintains a consistent response.

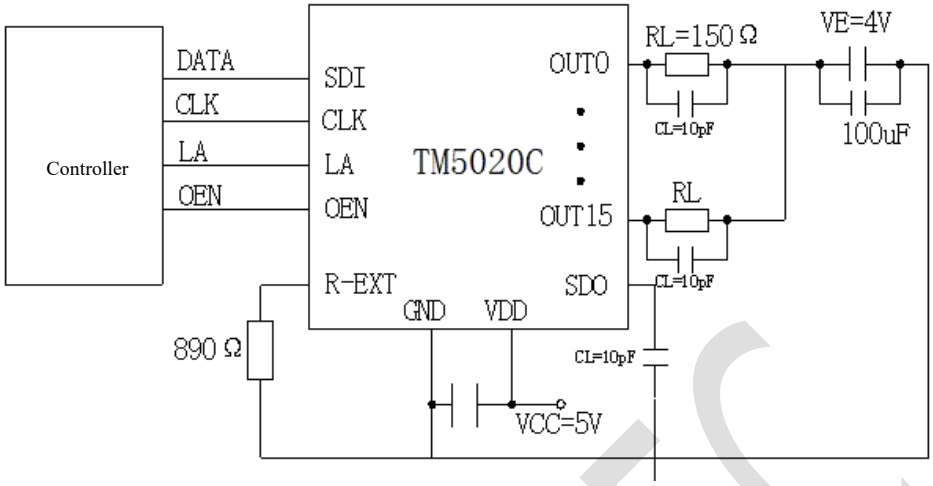
2) The delay time between even-numbered channels OUT2n (such as OUT0, OUT2, OUT4, OUT6, etc.) and odd-numbered channels OUT2n+1 (such as OUT1, OUT3, OUT5, OUT7, etc.) is 20nS. The TM5020C has a built-in delay circuit functionality, which can turn on the odd-numbered and even-numbered output channels at different times to reduce the amount of current in the power line.

11. Switching Features (VDD=3.3V)

Tested with VDD=3.3V and 25℃ except for other descriptions				TM5020C			Unit
Argument Name		Argument Symbol	Test Conditions	Min Value	Typ. Value	Max Value	
Delay Time (From Low Level to High Level)	CLK↑ - OUT2n↑	TPLH1	VDD=3.3V VDS=1.0V VIH=VDD VIL=GND REXT=930Ω VL=VE=3.0V RL=105Ω CL=10pF	——	35	55	nS
	CLK↑ - OUT2n+1↑			——	35	55	nS
	LE↑ - OUT2n↑	TPLH2		——	35	55	nS
	LE↑ - OUT2n+1↑			——	35	55	nS
	OE↑ - OUT2n↑	TPLH3		——	35	55	nS
	OE↑ - OUT2n+1↑			——	45	65	nS
	CLK↑ - SDO↑	TPLH		——	25	40	nS
Transfer Delay Time (From Low Level to High Level)	CLK↑ - OUT2n↓	TPHL1		——	35	55	nS
	CLK↑ - OUT2n+1↓			——	35	55	nS
	LE↑ - OUT2n↓	TPHL2		——	35	55	nS
	LE↑ - OUT2n+1↓			——	35	55	nS
	OE↓ - OUT2n↓	TPHL3		——	35	55	nS
	OE↓ - OUT2n+1↓			——	45	65	nS
	CLK↑-SDO↓	TPHL		——	25	40	nS
Pulse Width	CLK	TWCLK		20	——	——	nS
	LE	TWLE		20	——	——	nS
	OE	TWOE		50	100	——	nS
LE Setup Time	LE↓– CLK↑	TSU(L)		5	——	——	nS
LE Hold Time	LE↑– CLK↑	TH(L)		30	——	——	nS
SDI Setup Time	SDI – CLK↑	TSU(D)		3	——	——	nS
SDI Hold Time	SDI – CLK↑	TH(D)		5	——	——	nS
CLK Maximum Rise Time		Tr		——	——	500	nS
CLK Maximum Fall Time		Tf		——	——	500	nS
SDO Rise Time		Tr		——	10	——	nS
SDO Fall Time		Tf		——	10	——	nS
Potential Rise Time of Current Output		Tr		——	35	——	nS
Potential Fall Time of Current Output		Tf		——	50	——	nS

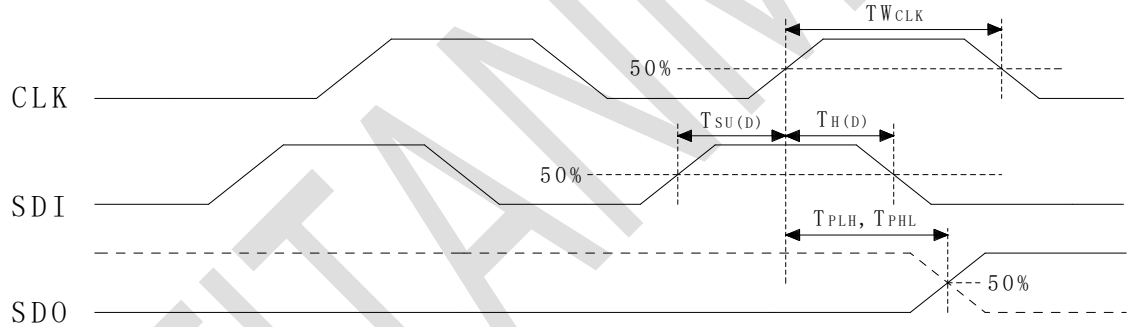
12. Test Curcuits of Dynamic Features

In order to avoid the influence of parity channels, the parity channel is independently connected to the power supply

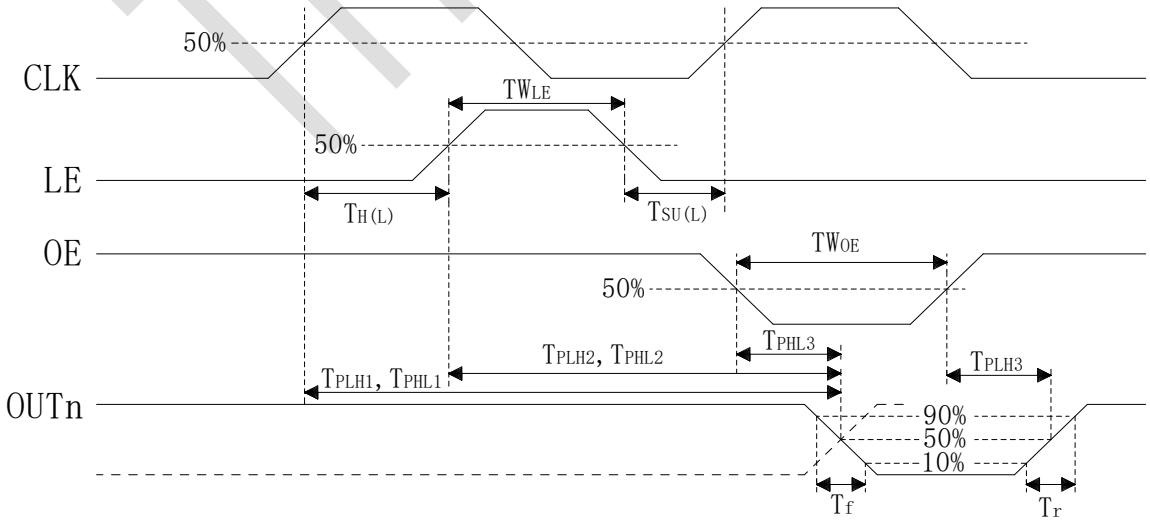


13. Sequence Diagram

1. Communication Timing

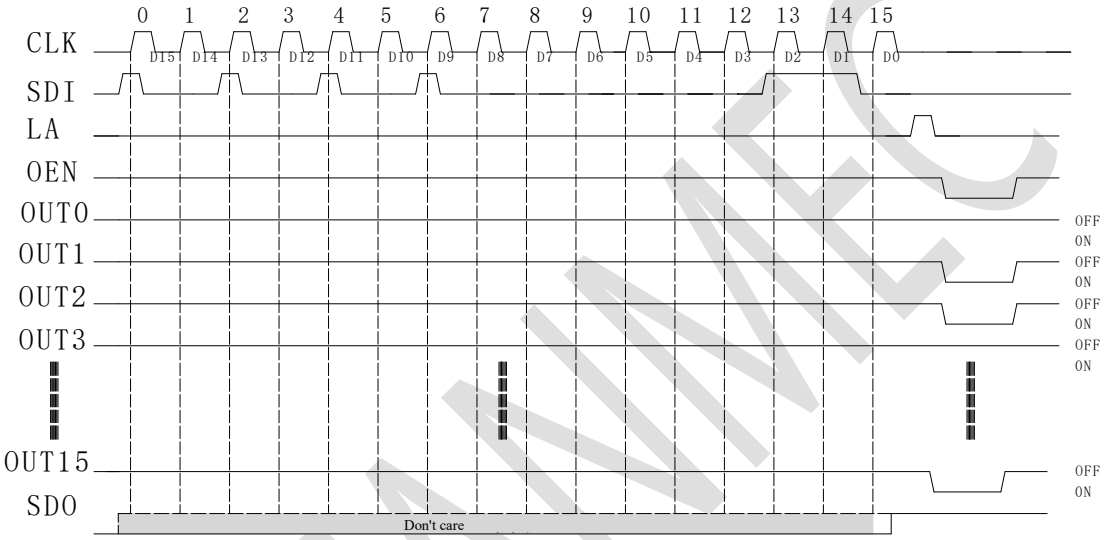


2. Channel Output Timing



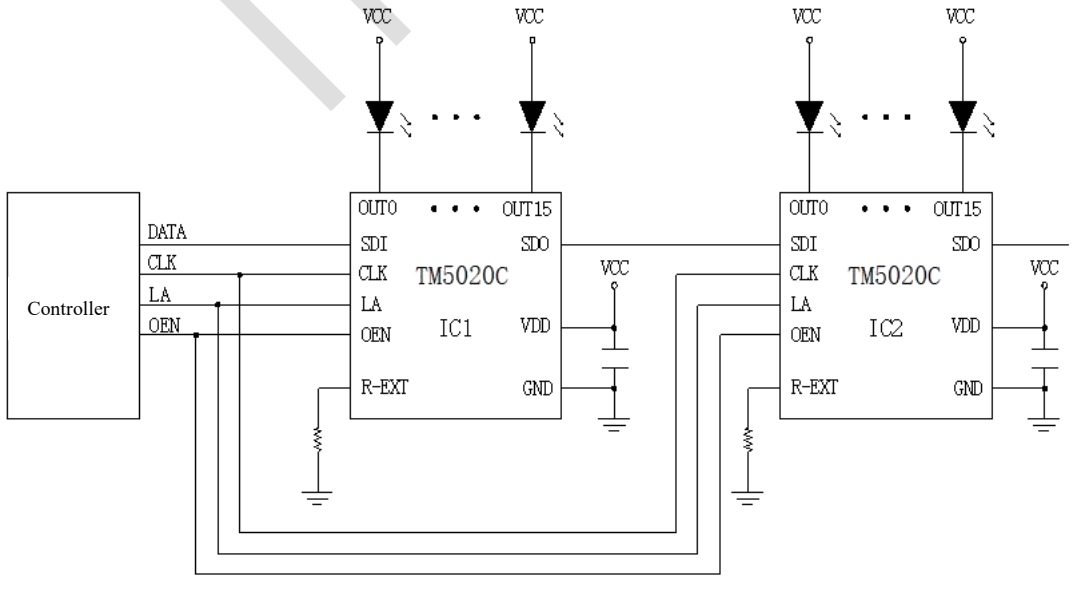
14. Logic Diagram

CLK	LE	OE	SDI	OUT0…OUT7…OUT15	SDO
↑	H	L	Dn	Dn … Dn－7 … Dn－15	Dn － 15
↑	L	L	Dn ＋ 1	No change	Dn － 14
↑	H	L	Dn ＋ 2	Dn+2 … Dn－5 … Dn－13	Dn － 13
↓	—	L	Dn ＋ 3	Dn+2 … Dn－5 … Dn－13	Dn － 13
↓	—	H	Dn ＋ 3	Off	Dn － 13



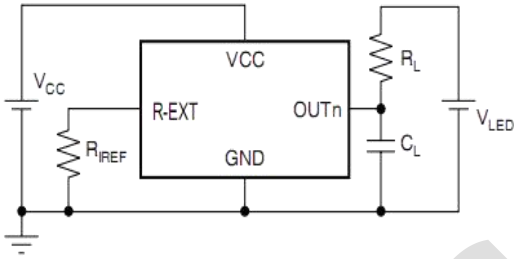
15. Application Information

Typical application diagram:



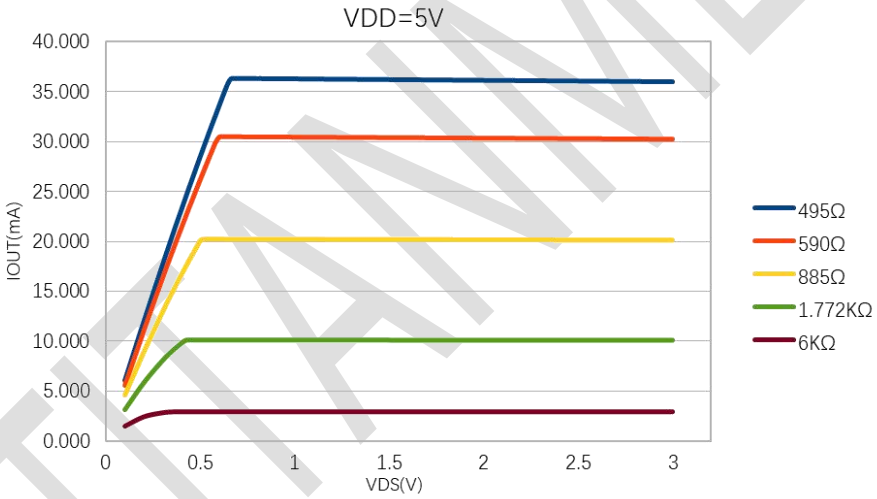
As shown in the following figure, the output current (I_{OUT}) is adjusted by an external resistor (Rext), and the output current value can be calculated by the following formula:

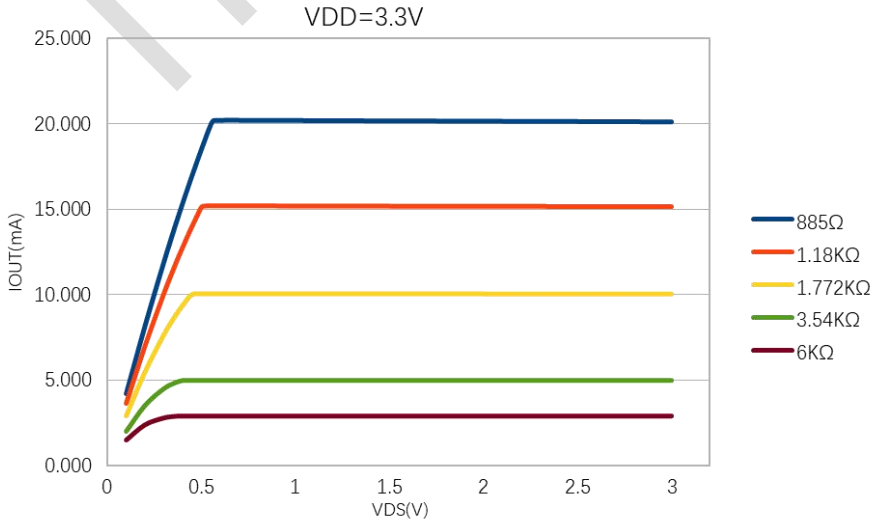
$$I_{OUT} = \frac{1.18V}{R_{IREF}} \times 15$$



R_{IREF} in the formula refers to the resistance of the R-EXT. When the resistance is 600Ω, the output current value is 29.5mA by the formula; when the resistance value is 1KΩ, the output current value is 17.7mA.

16. Constant Current



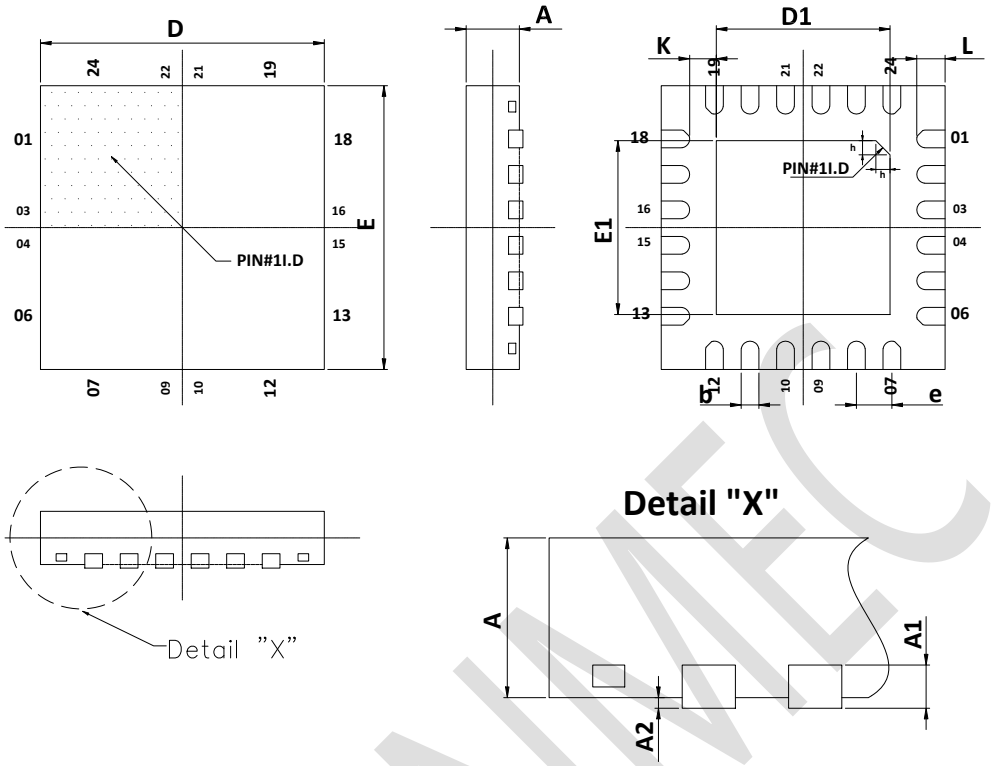


Connecting the R-EXT pin to GND with different resistance values can obtain different constant currents at the OUT pin output, but the voltage at the turning point of entering the constant current is different under different constant currents. As can be seen in the figure, the constant current voltage at 30mA ≈ 0.6V, and the constant current voltage drops to ≈ 0.5V at 20mA. When designing the circuit, the voltage drop at the OUTx should be fully considered to prevent the driver current from reaching the set value.

In addition, when the OUTx is turned on, it is not suitable to work on a high voltage drop for a long time, which will increase the chip power loss, which will cause serious chip heat and affect the system stability.

In practical applications, it may be caused by electromagnetic interference caused by signal wiring or other factors. To avoid such failures, it is recommended that the distance between TM5020C and the LED display module be as short as possible.

17. Package Conventional Diagram:QFN24



Dimensions

Item	D	E	D1	E1	A	A1	A2	b	e	K	L	h
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
Spec	4.10 (4.00) 3.90	4.10 (4.00) 3.90	2.55 (2.45) 2.35	2.55 (2.45) 2.35	0.80 (0.75) 0.70	0.213 (0.203) 0.193	0.05 (0.02) 0.00	0.300 (0.250) 0.200	0.500 YTP	0.385 (0.375) 0.365	0.50 (0.40) 0.30	0.250 (0.200) 0.150

All specs and applications shown above subject to change without prior notice.